Integrated Circuit Quality and Reliability
Second Edition, Revised and Expanded

Eugene R. Hnatek
Integrated Circuit Quality and Reliability
ELECTRICAL ENGINEERING AND ELECTRONICS
A Series of Reference Books and Textbooks

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Integrated Circuit Quality and Reliability
Second Edition, Revised and Expanded

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To my wife, Susan, for her patience, support, encouragement, and editorial help.

Additionally, I would like to publicly thank and praise the Lord Jesus Christ for His unconditional love, His faithfulness, His abundant grace and mercy, and for saving an unworthy sinner such as me through His death, burial, and resurrection.
The increased use of integrated circuits (ICs) in all types of products has been accompanied by a growing concern over IC failures. With the trend toward higher PC board complexity and the availability and use of denser ICs fabricated with new and complex process technologies, users have become increasingly concerned about inherent device quality. IC failures significantly impact a user's ability to do business in his chosen marketplace. What are the effects of device failures in the user's equipment? Equipment downtime, high warranty/repair costs, lawsuits, and loss of sales and goodwill. In the case of astronautics and aeronautics, repair might not be possible (e.g., a deep space probe that cannot be returned for repair, or an airplane that crashes), putting an extremely high price tag on the cost of a device failure, even to the point of loss of life. Consider an IC failure in computers that automate a steel manufacturing process, process banking transactions, or control the functioning of an automobile. The losses can be staggering, even immeasurable.

The semiconductor industry, by virtue of very-large-scale integrated "systems on silicon," is performing on a single chip the same function as the systems industry of yesterday. Consequently, the engineering, manufacturing
management, statistical quality assurance, and team concepts and methods
learned from the systems industry are being applied to the IC industry.

The words reliability and quality are often used interchangeably as though
they were identical facets of a product's merit; however, they are different.
Getting an exact and agreed-upon definition of quality is difficult. Quality
pertains to the population of faulty devices among the good ones as they arrive
at the user's plant (i.e., bad devices that escape the supplier's detection: Type
II errors). Some define quality as fitness for use. Others define it as conformance
to specifications. The quality of an IC can be defined as its performance in its
intended application. Quality is an inherent device characteristic that must be
both designed into the IC during circuit design, simulation, and process
development and manufactured in during wafer fabrication and assembly. Quality
is this and more. It is also determined by customer perceptions and expectations
and is what the customer gets out of a product and is willing to pay for.

Reliability is the probability that an IC will perform in accordance with
expectations for a predetermined period of time in a given environment. Thus,
reliability is quality on a time scale, so to speak, and testing (screening)
compresses the time scale. To meet any reliability objective requires a com­
prehensive knowledge of the interactions of the basic design, its inherent
weaknesses and sensitivities (failure mechanisms), and the application environ­
ment in which that design will operate.

Quality assurance historically has been an additive operation tacked on
after the completion of manufacturing to confirm that all steps were performed
properly via some means of inspection and/or testing. Quality assurance was
focused on the negative—catch the defects. It was predicated on the premise that
"you can't build it right." But this has changed due to the pressures of global
competition.

The focus has changed from the detection of defects to their prevention by
means of a proactive and aggressive approach to quality. In the past, methods
of increasing quality relied on testing. This was wrong on two fronts. First, you
can’t inspect or test quality into a product, and second, inspection personnel are
not solely responsible for quality; each individual in the organization is
responsible for quality. Thus, the way to produce a quality product is by
assembling a cross-functional team up front during product definition—repre­
senting design, package, process, software, and reliability engineering; manu­
facturing operations (wafer fabrication, assembly and test); and purchasing and
marketing—and by actively applying such techniques as design of experiments,
quality function deployment, design for manufacturability, design-for-test, and
design for reliability.

Testing and inspection are important in producing quality products. Testing
is the means by which data are gathered, analyzed, and fed back to design and
manufacturing for continuous improvement. In the past, electrical testing was
relied on heavily as a gate to check the quality level of outgoing parts and prevent the shipment of defective parts. During the past 14 years IC quality has dramatically improved due to a lot of hard work on the part of IC manufacturers. This began with a paradigm shift from a detecting-defects mindset to a preventing-escapes (zero-escapes) mindset as they embraced total quality management and applied problem-solving and statistical techniques to the design and manufacture of ICs. Final parametric electrical testing by the supplier is important to verify conformance to specifications, to grade products by classification, and to feed back the results of critical electrical parameter measurements and end-of-line defect information to manufacturing so they can correlate these measurements to process measurements, allowing continuous improvement to take place. But testing has aggressively moved forward into the wafer fabrication area in the form of process monitors or test structures immediately following each process step. This results in a short (if not instantaneous) feedback path, allowing real-time corrective action and improvement, reducing waste, rework, and cost. The application of statistical techniques in the wafer fabrication and assembly areas has been responsible for reducing defects from more than 10,000 parts per million a few years ago to fewer than 1000 parts per million today (averaged across all IC manufacturers, fabrication and assembly facilities, technologies, and product lines) and even below 100 ppm on a very specific supplier, technology, and product basis.

In order to understand IC quality, one has to know where defects can occur during design, wafer fabrication and assembly, and test. This requires an understanding of the IC technology as well as the potential failure mechanisms that can occur.

Since the first edition of this book was published, much has changed, and the pace of change and technological innovation will continue unabated. The section in Chapter 1 entitled "Trends" summarizes the significant changes. Yet much has remained the same. ICs have the same potential failure mechanisms as they did in the '60s, '70s, and '80s, but due to the circuit packing density and submicrometer geometries, they are much more susceptible to them than in the past. We are also faced with the issue of wearout mechanisms when dealing with vertical layer thicknesses measured in Angstroms, such as oxide wearout and electromigration wearout.

This edition has been updated and reorganized to reflect the changes that have taken place and add to the original baseline and tool set established in the first edition, yet it retains those elements that are fundamental to producing quality ICs irrespective of technological change.

The keynote address at the 1994 IEEE International Reliability Physics Symposium forecast that market factors (including huge capital costs) will make 100% yields a necessity for any semiconductor manufacturer to survive. In the future, he stated, defects are going to go away. This is a bold prognostication
indeed, considering the hundreds, if not thousands, of places in the IC design, wafer fabrication, assembly, test, and handling processes in which errors or defects can occur. One thing is certain: there will never be a dull moment. The future will be interesting, exciting, and extremely challenging. I look forward to it and hope that you do as well.

Eugene R. Hnatek
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Overview of Integrated Circuit Quality and Trends

HISTORICAL PERSPECTIVE ON IC QUALITY

The pace of industrial change has quickened during the past 14 years and will accelerate still further as America moves toward the 21st century. In the future, those companies that are keenly proficient at planning, implementing, and adapting to change will have a remarkable strategic advantage over their competitors. The basis of this proficiency will be flexibility in workers and managers, a less rigid corporate hierarchy, optimal use of technology, an emphasis on people, and widespread cooperation and teamwork within and outside of the organization—in essence, agile manufacturing.

Global competition has dramatically impacted the quality of products manufactured as measured by both customer expectations and satisfaction. Nowhere has change been so rapid, dramatic, or profound as in the U.S. semiconductor industry—specifically the design and manufacture of integrated circuits. Let’s step back and revisit what happened.

The American mass production paradigm tolerated, even expected, a certain amount of waste (faulty product) and used testing to remove that from the product shipped. Quality control by definition was dedicated to the premise that you can’t
get it right. Inspection reigned: both outgoing testing by the integrated circuit (IC) suppliers and 100% incoming inspection testing by the using community.

United States IC manufacturers had an essentially complacent attitude toward quality. In the 1960s and 1970s, IC suppliers often had a huge bone pile of reject devices at final electrical test. There was no concerted effort to find out the root cause of these rejects and institute a corrective feedback loop back to design and manufacturing. Further, it was found that a good percentage of these devices (30%–70%) were actually good parts but were failed (rejected) by the IC supplier's testing process. These are called Type I errors [1,2]. Also, during this time frame the users found a high percentage of rejects, as well, during their 100% incoming inspection testing. These were escapes from the IC supplier's final test area and are referred to in the literature as Type II errors [1,2].

These practices were brought to a screeching halt in 1980 when Hewlett-Packard dropped a bombshell. They announced that Japanese 16 K DRAMs exhibited one to two orders of magnitude less defects than did those same DRAMs produced by U.S.-based IC manufacturers. The Japanese aggressively and insightfully implemented the quality teachings (a.k.a. total quality management) of such visionaries as Drs. W. Edwards Deming and Joseph Juran and consequently forever changed the way that integrated circuits are designed, manufactured, and tested. Thus, the Japanese sounded a wake-up call to all of U.S. industry, not just the semiconductor industry, that shoddy quality products were not acceptable—they raised the bar for product quality and changed the focus from a domestic one to a global one.

The Hewlett-Packard announcement and subsequent loss of worldwide market share served to mobilize the U.S. IC industry and focus on quality to prevent its extinction (i.e., survival)—it stirred the U.S. IC industry from its complacency. The result was a paradigm shift from an inspection mindset to a genuine concern for the quality of ICs produced via a prevention or zero escape (i.e., a build it right the first time) mindset. It was simply a matter of design and produce quality ICs or go out of business.

Some of the factors fundamental and inherent to this paradigm shift include

• Quality is the sole responsibility of the IC supplier.
• Quality must be built and manufactured into the product, beginning at design.
• Design automation tools using accurate and continually refined models (logic simulation, process, fault simulation and grading, timing analysis, and testability analysis) are required for first-time functional success of a design.
• Use of cross-functional teams to apply design for manufacturability, design for reliability, design for test, design for packaging, and design of experiments techniques at the IC concept stage.
• Use of quality function deployment to aid in determining what the customer wants.
• Move testing farther up the IC manufacturing process, rather than being an end-of-the-line gate.
• On-chip test structures and process monitors are used by the IC supplier to monitor the wafer fabrication processes and make appropriate corrections/adjustments in essentially real time.
• The extensive use of continuous improvement statistical process control techniques has become a way of life for the IC supplier.

Since Hewlett-Packard’s 1980 announcement, U.S. materials, equipment, and IC manufacturers have worked feverishly to improve the quality of their materials and products. The improvement has been spectacular. As of this date, ICs produced by U.S. manufacturers are truly world class. Quality is no longer a differentiator, it is the table stakes required to get into the game. Thus U.S. IC manufacturers cannot stop their continuous quality improvement efforts. They must maintain their focus on quality.

Every person in the semiconductor industry must be dedicated to the production of quality products. Unless every person has that dedication, production yields and volumes quickly suffer, profitability drops, and company survivability soon becomes an issue. This requires formalized quality procedures and a company-wide quality mindset.

So much for historical perspective.

Now to the specific issues that affect IC quality. From a global IC design, manufacturing, and use perspective, sources of poor quality typically include and can be found

• In the design phase

  Process model errors/shortcomings
  No specifications
  Specification errors
  Improper and inadequate component characterization
  Design errors
  Inadequate design reviews

• In the manufacturing phase

  Material incompatibilities
  IC fabrication errors
  Wafer probe testing errors
  Packaging errors
  Packaged part testing errors
  Burn-in testing errors
• In OEM (original equipment manufacturer) construction phase

PCB assembly (soldering) errors
Processing damage
Fabrication errors
Acceptance testing errors
Board and system-level testing errors (timing errors!)
Handling (electrostatic discharge [ESD])
Improper part usage/application

• In field operation phase

Environmentally induced sources of error (temperature, radiation, vibration)
Voltage transients
Handling
Untrained personnel

According to IBM (E. Fishkill, N.Y.; personal communication), the two challenges in improving quality during processing are to improve the overall defect density of the product and to identify and eliminate "mavericks"—product that has been misprocessed and that has a significantly higher defect density and is inadvertently shipped to customers. Additionally, when dealing with the topic of IC quality one must consider more than the stand-alone IC. In today's environment one must view the IC and its total interconnection means to the PC board as an entity, a system if you will: the IC attachment to the PC board (i.e., solder joints); the PC board traces; the physical board layout and construction (ground planes, signal lines, cross-talk, power planes, electrical termination, thermal properties, etc.); PC board edge connectors and backplanes (board-to-board connection). This view must be taken because the IC is no longer the weakest link in system quality and reliability. Less than 5% of printed wiring assembly problems can be traced to the individual IC. The majority of problems are due to the following causes:

1. Connectors
2. Handling issues (mechanical damage, ESD)
3. PCB assembly problems (attachment to PCB, workmanship)
4. Solder joint integrity/reliability (attachment problems, mechanical support problems)

Why has the focus shifted from the individual IC to the total interconnection issue? The answer is severalfold:

1. ICs are of higher quality and more robust.
2. PC boards are more complex (multilayer with fine geometries).
3. The industrial environment is more severe.
This does not mean that we lessen our concern for IC quality. Quite the contrary. IC quality is the basis for system reliability and the focus of this book. The following chapters present the details of where errors occur in the IC wafer fabrication, assembly, and test processes and how they manifest themselves in the finished product.

Before we embark on the details of the IC quality journey, it is important to understand (1) the impact integrated circuits have on electronic product design and content and (2) the many changes (trends) that are shaping the IC industry complexion and will affect IC quality and reliability.

TRENDS

Electronics is important; it has literally transformed the world. It is the key ingredient of a nation's industrial and defense competitiveness and quality of life. In the United States electronics has become the largest manufacturing sector. Electronics continues to spin off new markets and industries as it grows, and it is integrated circuit technology that is the engine that drives all electronics-based and knowledge-based markets. Integrated circuit manufacturing is an enabling technology; i.e., it makes many things possible.

Figure 1.1 is a diagram that depicts the electronics food chain, beginning with the raw materials at the apex of the inverted pyramid and proceeding through to semiconductor equipment, to semiconductor manufacturing, and, finally, to electronic systems. Notice the multiplier (leverage) effect in going from raw materials and equipment to semiconductor manufacturing (almost 4×), and from semiconductor manufacturing to electronics systems (8×). This diagram dramatically illustrates the importance of electronics both in a nation’s economy and in the global economy.

IC Technology Acceleration

Developments in integrated circuit technology are proceeding at a rapidly accelerating pace. New technologies are supplanting existing ones faster than before, so much so that Texas Instruments officials have stated that, “New technologies are coming on-line so fast that we cannot adopt them in our new products fast enough.” (S. Golshan, Texas Instruments; personal communication).

The rapid changes taking place in integrated circuit design and technology development, and the pressure of bringing the resultant products to market rapidly, are bringing to bear fundamental changes in the thought processes of testing these circuits.

Testability must move forward to the circuit design stage and not wait until the design is fixed. As such, the circuit designer must address the issues of design-for-testability, built-in self-test, and fault coverage up front, on an equal-share-of-mind basis with the logic design.
This chapter presents some of the significant trends that are taking place in the IC industry and that will ultimately impact upon testability.

Table 1.1 summarizes the salient integrated circuit trends that are occurring. Each of these items will be substantiated by supporting data. ICs are advancing on two fronts simultaneously, almost paradoxically:

1. At the very-large-scale integration/ultra-large-scale integration (VLSI/ULSI) level with increased on-chip functional integration (memories, microprocessors, digital signal processors, and ASICS, for example).

2. At the small-scale integration/medium-scale integration (SSI/MSI) glue logic level with high performance (blazing speed <1 ns, and ultra-low power consumption).

Several examples are presented to show the increase in technology complexity. The first compares a 7400 bipolar transistor–transistor logic (TTL) NAND gate with a 256 K complementary metal oxide semiconductor (CMOS) static RAM:


Table 1.1 Integrated Circuit Trends

Technology is rapidly accelerating
- Greater functional density (complexity)—able to pack more into a smaller space.
- Higher operating speed (MHz, MIPS).
- Lower operating voltage (5 to 3.3 to 1.5 V).
- Larger IC package sizes due to increased use of I/O-intensive ASICs.
- More extensive use of ASICs and MCMs.
- The ability to effectively test, package, and remove the heat from state-of-the-art ICs will limit their growth and significantly impact upon equipment design.
- IC suppliers have stopped designing new logic families; building functions out of simple gates is no longer practical.

Higher quality products
- Application of concurrent engineering, design-of-experiments, design-for-manufacturability, design-for-reliability, and design-for-test practices at the inception of product development build quality into the product at the outset.
- Increasing importance of design automation to increase first-time silicon functional success by designing quality into the product.
- IC suppliers are moving to eliminate final electrical test. Instead, they use comprehensive, tightly guard-banded AC, DC, and functional tests at wafer probe. Final electrical test is used as a gross check for assembly defects.
- Increased use of process models for each wafer fabrication tool to reduce defects and increase first time silicon success; i.e., the need for extremely tight process control.
- Eliminate 100% incoming inspection and end-of-line testing.

Many designs with small manufacturing runs.
- Multiple sourcing of new devices is on the wane.
- Time is becoming a strategic weapon.
  - Decreasing product life cycles (2–4 years).
  - Shorter time to market.
- Product development costs are increasing geometrically such that no one company can go it alone. Thus, the proliferation of strategic alliances: design/manufacturing/foundry.
- Global dispersion of manufacturing.
- Increasing appearance of “fabless” IC suppliers.
- More services are outsourced than ever before as companies refocus on their “core” business.
- Increased incidence of elimination of non-profitable products, leading to obsolete and end-of-life parts issues.

<table>
<thead>
<tr>
<th>7400 NAND gate</th>
<th>36 transistors</th>
<th>60 contacts</th>
</tr>
</thead>
<tbody>
<tr>
<td>256 K SRAM</td>
<td>1.5 M transistors</td>
<td>4 M contacts</td>
</tr>
</tbody>
</table>

The second example compares 1970 state-of-the-art technology with 1989 state-of-the-art technology by number of mask steps and active layers:
<table>
<thead>
<tr>
<th>Year</th>
<th>Technology Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970</td>
<td>NMOS Technology</td>
<td>4 active mask steps, 20 major process activities</td>
</tr>
<tr>
<td>1989</td>
<td>Double metal CMOS</td>
<td>&gt;10 active mask layers, 50 major process activities</td>
</tr>
</tbody>
</table>

The third example of increased technology complexity is shown in the progression from SSI in the 1950s to VLSI circuits of the present time in Table 1.2.

Figure 1.2 compares feature size, metal layers, and unloaded gate delay for bipolar technology from 1978 to 1991. Also shown is a cross-section diagram of a 1991 state-of-the-art bipolar IC with four layers of interconnect (metallization). Figures 1.3, 1.4, and 1.5 show the increase in density trends for memories (1 K to 256 M) and microprocessors (4 bit to 32 bit), the increase in IC die size trends for the same memories and microprocessors, and the reduction in feature sizes for production as well as experimental circuits, respectively. From Figure 1.3 it is seen that memory density doubles every 3 years, memory die size increases by approximately 50% every 2.5 years (Fig. 1.4), and tight production memory feature size decreases at a rate of approximately 25% every 2 years (Fig. 1.5).

CMOS has become the primary technology for fabricating integrated circuits, moving from a small percentage (12%) of all ICs manufactured in 1982 to 82% forecast by 1996. Bipolar technology has become a special technology having flip-flopped with the percentage of CMOS ICs from 45% in 1982 to 50% of all projected ICs manufactured in 1997. These data are shown in Fig. 1.6.

VLSICs, due to their small geometries, have much higher operating frequencies and thus speeds. IC operating frequencies will increase in the manner shown in Fig. 1.7. In fact, digital ASICs and VLSICs look like radiofrequency (RF) circuits, and must be treated as such, with proper transmission line termination, cross-talk protection, and grounding, for example.

Then, too, the operating voltage is being reduced due to both the physical limitations of materials used to manufacture ICs and the high levels of integration being achieved. Specifically, the smaller geometries required for start-of-the-art ICs (i.e., 64 Mb, 256 Mb, and 1 Gb DRAM) require lower power supply voltages, due to the dielectric and metallization thickness issues and transistor breakdown characteristics. The portable personal computer is driving the trend toward reduced operating voltage, going from 5 V to either 3.0 or 3.3 V now, and eventually to 1.5 V. This change (5.0 to 3.3 V) will double the battery life by reducing power dissipation. However, as the voltage is reduced, the operating speed (frequency) is reduced, the devices become more sensitive to static discharge handling, and there are smaller noise margins. All of this means that special care will be required when handling lower voltage ICs during equipment manufacturing.
<table>
<thead>
<tr>
<th>Dates</th>
<th>Integration level</th>
<th>Number of transistors</th>
<th>Equivalent gates</th>
<th>Typical functions or systems</th>
<th>Typical number at I/Os</th>
</tr>
</thead>
<tbody>
<tr>
<td>1950</td>
<td>SSI</td>
<td>1–40</td>
<td>1–10</td>
<td>Single circuit function (e.g. transistors)</td>
<td>14</td>
</tr>
<tr>
<td>Late 1960s</td>
<td>MSI</td>
<td>40–400</td>
<td>10–100</td>
<td>Functional network</td>
<td>24</td>
</tr>
<tr>
<td>Late 1970s</td>
<td>LSI</td>
<td>40–4500</td>
<td>100–1000</td>
<td>Hand calculator or digital watch</td>
<td>48</td>
</tr>
<tr>
<td>Mid 1980s</td>
<td>VLSI</td>
<td>4500–300,000</td>
<td>1000–80,000</td>
<td>Microprocessors</td>
<td>64–300</td>
</tr>
<tr>
<td>Present</td>
<td>ULSI</td>
<td>Over 300,000</td>
<td>Over 80,000</td>
<td>Computer on a chip</td>
<td>200–400</td>
</tr>
<tr>
<td>Year</td>
<td>Feature size (μ)</td>
<td>Metal layers</td>
<td>Process keys</td>
<td>Unloaded gate delay</td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>------------------</td>
<td>--------------</td>
<td>--------------------------------------------------------------------------------</td>
<td>---------------------</td>
<td></td>
</tr>
<tr>
<td>1978</td>
<td>4</td>
<td>1</td>
<td>Oxide isolation with diffused junction</td>
<td>5–10 ns</td>
<td></td>
</tr>
<tr>
<td>1980</td>
<td>3</td>
<td>1</td>
<td>Oxide isolation with implanted junction</td>
<td>1–5 ns</td>
<td></td>
</tr>
<tr>
<td>1981</td>
<td>2</td>
<td>2</td>
<td>Oxide isolation with implanted junction</td>
<td>500–700 ps</td>
<td></td>
</tr>
<tr>
<td>1983</td>
<td>1.5</td>
<td>2,3</td>
<td>Oxide isolation with implanted junction</td>
<td>300–500 ps</td>
<td></td>
</tr>
<tr>
<td>1985</td>
<td>2</td>
<td>3</td>
<td>Poly emitter and resistors, silicide interconnect</td>
<td>70–150 ps</td>
<td></td>
</tr>
<tr>
<td>1988</td>
<td>1.5</td>
<td>3</td>
<td>Poly emitter and resistors, silicide interconnect</td>
<td>50–70 ps</td>
<td></td>
</tr>
<tr>
<td>1991</td>
<td>0.8</td>
<td>4</td>
<td>Poly emitter and resistors, silicide interconnect, stepper or direct-write lithography</td>
<td>10–50 ps</td>
<td></td>
</tr>
</tbody>
</table>

Advances in ECL Technology

Figure 1.2  (a) Bipolar IC technology summary. (b) Schematic cross section of a typical interconnect structure.

The low operating voltage road map that has been plotted is as follows:

- 64 Mb DRAM    3–3.3 V
- 256 Mb DRAM   2.5 V
- 1 Gb DRAM     1.5 V
What kind of protective packages will be required to house these die? Since about 1984 a fundamental transformation has been occurring in earnest, from through-hole insertion packages (dual-in-line packages) to surface-mount packages (quad flat pack, leadless chip carrier, small outline J lead, etc.). Surface-mount technology (SMT) will grow from 44% in 1993 to 75% of all packages by 1998, as shown pictorially in Figure 1.8, being led by the small outline integrated circuit/small outline J-lead (SOIC/SOJ) and plastic leadless chip carrier/plastic quad flat package (PLCC/PQFP) package styles (Table 1.3). The change to SMT packages impacts upon handling during PC board assembly,
leading to a host of quality and reliability usage issues. With surface mount technology, ICs can no longer be viewed individually, but rather must be considered in conjunction with their mounting on the PCB board and the solder as a system.

Adding to the package style transformation is the rapid increase in the number of external package leads (or pins). Figure 1.9a illustrates the dramatic growth trend in pin count from 68 in 1980 to 512 in 1990. Figure 1.9b shows the pin count trend for memories, microprocessors (MPUs) and ASICs, historically from 1960 to the beginning of the century. Integrated circuit packages with pin counts of 900 to 1000 will be in production by the year 2000. Larger package sizes (measured by the number of leads) are required to accommodate large die sizes (as was shown in Figure 1.4), especially of application-specific integrated circuits (ASICs) which are input/output (I/O) intensive (versus memories), and which make less efficient use of silicon real estate. Figure 1.10 shows the trends

**Figure 1.4** Integrated circuit die size trends. (Courtesy of ICE Corp., STATUS 1994.)
relating the number of signal pins to the gate count. Memories, being orthogonal structures, have the lowest I/O pin count versus gate count; gate arrays (ASICs) have the highest. Table 1.4 shows the gate-to-I/O pin ratio for microprocessors.

The large number of leads had led to a shift to smaller (fine pitch) lead spacings (50 to 25 to 10 mil) and a corresponding increase in testing and handling (lead damage), assembly, and electrical performance (cross-talk, ringing, and spurious noise) problems. The high gate (or transistor) counts per IC demand innovative packaging techniques such as the use of multichip modules (MCMs) to increase system performance and decrease size. MCMs, and the ASICs and VLSICs that constitute MCMs, present some serious test problems. Figure 1.11 depicts the relationship between increased gate count, increased pin (lead) count, and viable package style: dual-in-line package, quad flat package, pin grid array, and MCM.

All of the aforementioned technology trends lead one to the following conclusion—the growth of VLSI (including ASIC) and ULSI circuits will be limited by (1) the ability to package the devices, (2) the ability to effectively remove internally generated heat from the chip–package combination, and (3)
Figure 1.6  1982–1998 IC technology trends and projected trends. (Courtesy of ICE Corp., STATUS 1994.)

Figure 1.7  Growth in device speed.
the ability to properly test the devices, thus significantly impacting upon equipment/product design, performance, quality, and reliability.

Electrical testing of very-large-scale and ultra-large-scale integration devices may account for as much as 45% of total product costs (Fig. 1.12), and these costs may escalate as VLSI and ULSI devices continue to shrink.

Table 1.3  Industry Usage of IC Package Styles

<table>
<thead>
<tr>
<th>Package type</th>
<th>1993 Units (M)</th>
<th>1993 Percent of total</th>
<th>1998 Units (M)</th>
<th>1998 Percent of total</th>
<th>1993–1998 CAGR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic dip</td>
<td>21,350</td>
<td>52</td>
<td>12,900</td>
<td>23</td>
<td>-10</td>
</tr>
<tr>
<td>Cerdip</td>
<td>1300</td>
<td>3</td>
<td>725</td>
<td>1</td>
<td>-11</td>
</tr>
<tr>
<td>Sidebraze dip</td>
<td>50</td>
<td>&lt;1</td>
<td>35</td>
<td>&lt;1</td>
<td>-7</td>
</tr>
<tr>
<td>Ceramic PGA(^a)</td>
<td>175</td>
<td>&lt;1</td>
<td>280</td>
<td>&lt;1</td>
<td>10</td>
</tr>
<tr>
<td>Plastic PGA(^a)</td>
<td>150</td>
<td>&lt;1</td>
<td>675</td>
<td>1</td>
<td>35</td>
</tr>
<tr>
<td>SOIC(^b)</td>
<td>8100</td>
<td>20</td>
<td>19,410</td>
<td>34</td>
<td>19</td>
</tr>
<tr>
<td>SOJ</td>
<td>2300</td>
<td>6</td>
<td>9560</td>
<td>17</td>
<td>33</td>
</tr>
<tr>
<td>PLCC</td>
<td>4175</td>
<td>10</td>
<td>6300</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>PQFP</td>
<td>1725</td>
<td>4</td>
<td>4200</td>
<td>7</td>
<td>19</td>
</tr>
<tr>
<td>LLCC/LDCC</td>
<td>375</td>
<td>1</td>
<td>515</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>Other(^c)</td>
<td>1000</td>
<td>2</td>
<td>2400</td>
<td>4</td>
<td>19</td>
</tr>
<tr>
<td>Total</td>
<td>40,700</td>
<td>100</td>
<td>57,000</td>
<td>100</td>
<td>7</td>
</tr>
</tbody>
</table>

\(^a\)Includes ball grid arrays (BGAs).
\(^b\)Includes UTSOPs, QSOPs, and TSOPs.
\(^c\)Includes TAP-on-board, COB, flatpacks, metal cans, etc.
Figure 1.9  (a) Package pin count growth trends. (b) Pin count trends for memories, microprocessors, and ASICs. (Courtesy of ICE Corp., STATUS 1994.)
Overview of IC Quality and Trends

Figure 1.10 I/O pin count versus complexity. (Courtesy of ICE Corp., STATUS 1993.)

Table 1.4 The Growing Gate-to-I/O Pin Count Ratio: Microprocessor (μP) Size Versus Pin Count

<table>
<thead>
<tr>
<th>μP</th>
<th>Word size (bits)</th>
<th>Manufacturer</th>
<th>Approximate no. of transistors</th>
<th>Pin count</th>
<th>Gate/pin ratioa</th>
</tr>
</thead>
<tbody>
<tr>
<td>4004</td>
<td>4</td>
<td>Intel</td>
<td>2,300</td>
<td>16</td>
<td>48</td>
</tr>
<tr>
<td>6800</td>
<td>8</td>
<td>Motorola</td>
<td>4,000</td>
<td>40</td>
<td>33</td>
</tr>
<tr>
<td>8085</td>
<td>8</td>
<td>Intel</td>
<td>15,000</td>
<td>40</td>
<td>125</td>
</tr>
<tr>
<td>8086</td>
<td>16</td>
<td>Intel</td>
<td>29,000</td>
<td>40</td>
<td>242</td>
</tr>
<tr>
<td>WE32100</td>
<td>32</td>
<td>Bell Laboratories</td>
<td>180,000</td>
<td>132</td>
<td>341</td>
</tr>
<tr>
<td>68020</td>
<td>32</td>
<td>Motorola</td>
<td>200,000</td>
<td>114</td>
<td>439</td>
</tr>
<tr>
<td>80386</td>
<td>32</td>
<td>Intel</td>
<td>275,000</td>
<td>132</td>
<td>521</td>
</tr>
<tr>
<td>HP9000</td>
<td>32</td>
<td>Hewlett-Packard</td>
<td>450,000</td>
<td>83</td>
<td>1350</td>
</tr>
</tbody>
</table>

aGate/pin ratio was estimated using four transistors per gate in CMOS technology and three transistors per gate for nMOS and pMOS technology.
Figure 1.11  Package style trend chart as a function of gate and pin counts.

Figure 1.12  Very-large-scale IC test development costs swamp product design and development costs. Test development effort increases as a percentage of total device development costs of next-generation IC technology.
The Issue of Quality

In today's environment quality is not an issue. It is a given! The starting point to participating in the global marketplace is a high-quality product as determined by the user (customer). Thus, quality is the price (table stakes if you will) of getting into the game, and to stay in the game, a total quality system based on a continuous quality improvement process must be put into place. Quality is the never-ending driving force to competitiveness.

Quality must be designed and built into the product at the outset. One cannot wait until the IC is manufactured and then use testing to provide a "good" product. Quality must be built into the IC by assembling a multi-disciplined design team that jointly addresses design, manufacturability, fault coverage, testability, and reliability issues before the design begins, throughout the design process, and then carrying on right into the production stage. This process is aided by the availability of capable design automation tools in conjunction with accurate and continuously refined logic and process model libraries.

In the early 1960s, it was indeed rare that one obtained first-pass working (functional) silicon for even a simple device such as a 7404 logic device. However, with currently available design automation tools, first-time functional silicon is obtained almost 100% of the time with such complex circuits as megabit memories, 32-bit microprocessors, and ASICs. This happens because a given integrated circuit, by virtue of these computer-aided tools,

- Is "debugged" before it is ever manufactured (via logic simulation, timing analysis, design rules check, and layout analysis)
- Has its fault coverage and testability established up front during circuit design by the implementation of design-for-test (DFT) and built-in self-test circuitry and techniques
- Has eliminated costly hit-and-miss design-fab-design-fab iterations
- Has the test strategy and production test vector set developed during IC circuit design

Because of this concern for quality in conjunction with the evolution of design automation tools, there has been a dramatic improvement in the quality and reliability of integrated circuits during the past 10 years (see Fig. 1.13). But, quality improvement is never over. It is a never-ending daily task—to continuously improve and make higher quality ICs.

Electrically Testing ICs

As was both stated and alluded to earlier, electrically testing an integrated circuit is a complex issue compounded by the many technological trends simultaneously taking place. In this small section I just want to emphasize two points, since a
Figure 1.13  Trends in reliability goals. Circles, long-term failure rate goals (FIT); squares, infant mortality goals (DPM).

later chapter (Chapter 8) discusses the issues of testing VLSICs and ASICs in greater detail.

1. As device complexity increases, fault coverage decreases, requiring the use of design-for-test (DFT) techniques.
   a. On-chip test structures.
   b. On-chip circuits incorporating boundary scan or level-sensitive scan design (LSSD) to ease testing.

2. A transformation in electrical testing of VLSICs and ASICs is occurring. Test generation is moving closer to and becoming a part of the design environment (i.e., integrated design and test).

Other Trends

In the 1960s and 1970s, the integrated circuit industry was characterized by a small number of standard products manufactured in high volume: 100 or so standard products (designs) each with an average of 500,000 devices manufactured. With the availability of design automation tools to virtually everyone (especially systems designers), and the establishment of silicon foundries and third-party design houses, the integrated circuit industry has changed such that it is now characterized by thousands of designs with small manufacturing "runs" (200 or so devices on average). This change is shown in Fig. 1.14. Thus, the industry has seen a major shift from a small number of high-volume parts to a large number of small-volume parts. Compounding the issue is that many of the
thousands of designs will never get to production. The designs and operating functions are being changed, modified, upgraded, or dropped altogether. Nonetheless, these devices need to be electrically tested. Are the parts "good"? To what specifications? How "good" are they? Will they work in my application? Test vectors must be developed rapidly to support the manufacturing/production function, thus putting much stress on both the circuit designer and test engineer.

Lastly, there is the issue of time. IC design cycles are decreasing. This, plus the complexity of ICs and the development costs, requires cost-sharing partnering arrangements to bring out products rapidly. Time is a twofold issue. Product life cycles (both ICs and equipment) are decreasing rapidly. Generally speaking, glue logic ICs have a life of 7 years, memories 5 years, microprocessors 3–7 years, and ASICs 1 year or less. Then there is a shorter time to market. IC suppliers must bring out even more complex IC designs at an ever increasing rate, yet the development cost of these designs is accelerating at a rate typified by the following example:

8086 Microprocessor $25M
80386 Microprocessor $100M
80486 Microprocessor $250M

A 1–2 calendar-year time to market is not uncommon for VLSI circuits. Because of these time pressures, coupled with the competitive nature of the industry, the IC suppliers must recover their design and process development and test development costs up front.

Not only are the IC suppliers faced with shorter prototyping and product release times, but they must bring the IC to market when scheduled or incur a serious profit shortfall as shown in Fig. 1.15. Thus, time-to-market is critical because it affects both market share and profit.

Both of these issues of time place enormous stress on test strategy
development. For complex devices, the IC suppliers simply cannot test for all possible usage conditions (Intel’s 80486 microprocessor, for example). What we are coming to is the need for application-specific testing. However, the issues are the same. The IC suppliers cannot afford to fail good devices in their electrical test areas (Type I errors), since this increases their costs and all users must pay for these, nor can they pass bad devices (Type II errors) to the user since a given user will pay for these parts. In both cases the IC supplier’s reputation will suffer and it will lose its market share.

Thus, in summary, the many IC technology trends taking place will have a significant impact on the failure mechanisms encountered, testability, quality, application usage, and reliability.

REFERENCES

Part I

Introduction to Integrated Circuit Manufacturing Processes

In the IC industry change is the norm. Circuit design and wafer fabrication processes are being changed, modified, and innovated to increase both the electrical performance characteristics and producibility (yield) of finished ICs. Memories (DRAMs, SRAMs, EPROMs, Flash), are the vehicles used to demonstrate and refine new and/or modified processes by virtue of their high production volumes and repetitive on-chip structures where asset (equipment) utilization and lowest cost are important. They are process drivers. Application-specific ICs (ASICs) are technology drivers that demonstrate new and/or modified designs where cycle time is important. Once these design and process innovations are refined, they filter downward to all areas involving mature products that may be restructured, redesigned, or resteped for large wafer sizes—or a combination of all of these—in order to decrease die size, obtain more die per wafer, decrease the cost per die, and increase profits and inherent device quality levels.

At the same time, users have become more concerned about inherent device quality because of higher printed circuit board (PCB) densities, and the availability and use of dense very-large-scale integration (VLSI) devices fabricated with new and complex process technologies. The failure of a VLSI device
Figure 1.1 Integrated circuit manufacturing process overview.
in a circuit board has a much more pronounced effect on the end-equipment operation than did a simple gate failure in prior generations of the equipment design. Thus, the increased use of both integrated circuits and VLSI circuits in electronic systems has been accompanied by an increased concern over IC rejects and IC quality.

In this section, the IC manufacturing process is discussed solely from a perspective that details the factors in this process that affect the finished IC quality, rather than from a theoretical design perspective. Up front it must be stated that everything in an IC is in an unstable environment as a result of the complex chemical makeup and physics of materials interactions (on an atomic particle level) that come into play in the fabrication and assembly processes. The materials want to diffuse into each other—silicon into the bonding wires; aluminum from bonding wires into the package and die attach pads; oxygen from the cavity into silicon; moisture and contaminants in the cavity, and the like. These factors are affected and accelerated by time and temperature conditions and impact device quality.

Although several typical wafer fabrication (process) sequences are presented, they are to be considered as generalized examples to demonstrate to the reader the steps involved in making an IC and are subject to much variation from supplier to supplier as the state of the art changes. The various processing steps discussed are valid in and of themselves, but when combined to form the total process may vary in where they fit into the sequence, if they are used at all, or in how many times each step is used in a given process. Furthermore, there is much variation within each processing step from supplier to supplier and among the product lines of a given supplier, such as the length of time and the temperature under which impurities are diffused into a wafer.

Figure 1.1 presents a global overview of the integrated circuit manufacturing process which greatly simplifies its inherent complexity but serves to highlight the salient process steps for the reader.
Front-End IC Fabrication Operations

The IC manufacturing process involves the disciplines of chemistry, physics, materials science, thermodynamics, and statistics in a complex interrelationship in front-end (wafer fabrication) and back-end (assembly and test) operations.

**BASIC IC MATERIALS**

Semiconductor materials are crystalline, with a simple physical and chemical structure. They are neither good conductors of electricity nor good insulators. While there are many semiconducting compounds and elements, silicon is the primary material for ICs. Monocrystalline silicon in its pure, intrinsic form exhibits few useful properties. However, the carefully controlled addition of trace amounts of specific impurities to “dope” the silicon makes it possible to alter its characteristics in an extremely useful manner.

Semiconductor-grade silicon is refined from common beach sand. This is reduced to polycrystalline high-purity silicon in the form of long, slender rods. These rods are then changed to single-crystal silicon by means of either the Czochralski (CZ) or the float-zone method. A new development, magnetically
grown Czochralski (MCZ) silicon crystals, has been shown to have lower defect densities and less warpage than conventional CZ silicon. MCZ also has been found effective in linearizing oxygen defects through the crystal rather than allowing the concentration at the seed end that has typified earlier silicon, resulting in low leakage currents.

The resultant crystals are then ground to a uniform diameter with diamond grinding equipment. Each crystal is sawed into thin slices, or wafers. These wafers, which are as brittle as glass and are between 10 and 20 mils thick, are etched and lapped on both sides to remove any structural damage that might have occurred during sawing. Wafers that will be used to make ICs are then polished to a mirror finish on one side.

After polishing, the wafers are thoroughly cleaned. Cleaning involves solvent degreasing using heated detergent solutions under ultrasonic agitation and wiping. The final cleaning is often chemical etching. This produces a wafer suitable for use in manufacturing integrated circuits. Most IC suppliers buy prepared wafers (in 5-in., 6-in., and 8-in. diameters) of silicon ready for the first manufacturing step with the desired resistivity.

The crystalline structure (lattice) of silicon is basic to semiconducting action. Pure silicon at room temperature is a poor conductor of electricity because each atom in the crystal has four other silicon atoms around it, which in turn are bound to four neighboring atoms, and so on. So all the outer electrons in a perfect silicon crystal are linked and are not available to conduct electricity, if the effects of temperature are ignored.

Due to thermal energy, however, at any temperature above absolute zero (0°K), some of these relatively weak covalent bonds are broken, where the number of such broken bonds is a function of the temperature. Broken bonds free the electrons involved, which are then available to conduct electricity. Similarly, broken bonds corresponding to the absence of an electron (known as a "hole") are free to move through the crystal lattice. The electrons are negative charge carriers, while the holes comprise, in effect, positive charge carriers (absence of an electron). (One can consider the holes as analogous to bubbles in a liquid, in which the bubbles, which are actually the absence of liquid, are free to move through the liquid.) Both types of charge carriers are capable of conducting an electric current—or, more precisely, their ordered movement may comprise an electric current. However, if other elements are introduced as substitute atoms into the silicon crystal lattice, the electrical properties of silicon can be altered in a controlled manner. The substitution of "dopant" atoms that are appropriate for this purpose are certain members of Groups III and V of the Periodic Table of Elements (see Appendix) that contain three and five valence electrons, respectively. Among the Group III elements that have been used to dope silicon are boron, gallium, and indium. Probably the most widely used of these is boron, which has only three electrons in its outermost orbit.
When boron is present in the crystal lattice, it is deficient by one electron of the four needed for covalent bonding with neighboring silicon atoms. To provide the missing fourth electron, it accepts one, thereby producing a hole (corresponding to the absence of the electron it accepted). The Group III elements are known as “acceptors,” their presence in the silicon crystal lattice produces p-type silicon, and they conduct by means of positive charge carriers (holes).

Conversely, elements in Group V of the Periodic Table that contain five electrons in their outermost orbits (e.g., phosphorus) are known as donor elements. In the silicon crystal lattice, when they share electrons with their nearest neighbors only four electrons are needed, leaving one unused electron. This electron is then free to carry current. When silicon is doped with donor atoms, it is known as n-type silicon, and conduction occurs by negative charge carriers (the free electrons).

**Doping Silicon**

Active circuit elements such as metal oxide semiconductor (MOS) transistors and bipolar transistors are formed in part within the silicon substrate. To construct these elements it is necessary to selectively introduce impurities, that is, to create localized n-type and p-type regions by adding the appropriate dopant atoms.

The process of introducing controlled amounts of impurities (Group III or Group V atoms) into the lattice of monocrystalline silicon is known as *doping*. Basically, an appropriate compound of the desired element (very often its oxide) is deposited on the surface of a silicon wafer, which is subjected to elevated temperature. The dopant then diffuses into the silicon. As long as there is an excess of dopant present on the silicon surface, the surface concentration of these atoms in the silicon will be determined by the solid solubility of the element in silicon, which is a function of temperature alone. Maximum solid solubilities of typical silicon dopants range from $5 \times 10^{20}$ atoms/cm$^3$ for boron through $1.4 \times 10^{21}$ atoms/cm$^3$ for phosphorus, and up to $1.8 \times 10^{21}$ atoms/cm$^3$ for arsenic.

The elements that are used as dopants are impurities only in the sense that they represent a departure from pure silicon crystal. The silicon itself is very pure, as are the dopant elements. In fact, silicon is the purest raw material ever produced in large quantities. Impurity levels of one part or less per billion are common.

Dopant elements may be added to the silicon at several points in the IC manufacturing process as will be discussed in the balance of this chapter. The effects of dopants give silicon nearly any desired resistivity, and either p- or n-type conductivity. The boundary between a p-type region and an n-type region is called a p-n junction. The active portion of a semiconductor device consists of p- and n-type regions and the junctions between them.

The dominant role of silicon as the material for integrated circuits is attributable in large part to the properties of its oxide. Silicon dioxide is a clear
glass with a melting point higher than 1400°C. It plays a major role both in the fabrication of silicon devices and in their operation. The combination of desirable properties of SiO$_2$ is unique. SiO$_2$ is stable in a wide range of ambient environments, and a high-quality film can be conveniently grown on single-crystal silicon by means of thermal oxidation.

**IC DESIGN**

The structure of an integrated circuit is complex both in the topography of its surface and in its internal composition. Each element of a IC has an intricate three-dimensional architecture that must be reproduced exactly in every circuit. The structure is made up of many layers, each of which is a detailed pattern. Some of the layers lie within the silicon wafer and others are stacked on the top. The manufacturing process consists of forming this sequence of layers precisely in accordance with the plan of the circuit designer.

Before examining how these layers are formed it will be helpful to take an overall look at the procedure by which an integrated circuit is transformed from its conception, by the circuit designer, to a physical reality.

Circuit design starts with a functional block diagram or description of how the circuit must operate. This block diagram shows the operation of the circuit without any of the design specifics. The circuit designer is concerned with the electrical functions of the finished device or circuit parameters and then designs the individual on-chip semiconductor components required to produce the desired circuit function. The circuit designer also selects the processing steps that will be required to manufacture the circuit. Next, the actual design of the IC begins. The size and approximate location of every circuit element are estimated. Much of this preliminary design work uses computer-aided design (CAD), with the aid of engineering workstations that can simulate the operation of the circuit without actually physically constructing the circuit in much the same way that electronic television games simulate the action of a table-tennis game or a space war. The circuit designer monitors the behavior of the circuit voltages, using a logic simulator, and adjusts the circuit elements until the desired behavior is achieved.

The inputs to the logic simulator are the assembled network description and a sequence of design verification tests, either supplied by the customer or developed by the supplier. The computer applies this sequence of tests to the input of the assembled network. When simulation is complete, a printout of the logic states of inputs, outputs, and selected internal points as a function of time is obtained. In essence, the computer is performing a function similar to breadboarding the circuits but in this case a more concise picture of the circuit response versus time is achieved. A study of the simulation printout is made to verify the correctness of the stored network.

After the stored network is verified, a propagation delay program estimates
the capacitance associated with each node in the network and calculates the
propagation delay through each logic gate. The designer analyzes this infor-
mation for possible speed problems and determines which interconnection paths
must have minimum capacitance. When the chip layout has been completed,
the exact node capacitances are automatically computed, based upon layout
information. The results are reexamined as a final check for proper AC
performance.

Computer simulation is less expensive than assembling and testing a
“breadboard” circuit made up of discrete circuit elements; it is also more accurate.
The main advantage of simulation, however, lies in the fact that the designer
can change a circuit element merely by typing in a correction on a keyboard,
and can immediately observe the effect of the modification on the behavior of
the circuit. The topic of circuit design for VLSI circuits using engineering
workstations is discussed in greater depth elsewhere in this volume.

Figure 2.1 is a schematic diagram of a 709 operational amplifier as an
illustrative example of a completed IC schematic design. This is a very simple
and archaic IC measuring 38 × 38 mils but is useful for showing the different
masking steps.

Once the designer is satisfied with the circuit simulation, the automatic
circuit layout (transforming the circuit schematic diagram to a physically
realizable topographical implementation), namely, the artwork generation, giving
the precise position of the various circuit elements, begins. Either the designer
calculates the physical dimensions required to produce the desired electrical
parameters or the information is stored in the computer (the design data base)
and the CAD system determines the circuit elements that will be used. Typically,
the vertical dimensions determine diffusions, chemical vapor deposition (CVD),
and doping thickness specifications. The horizontal dimensions determine the
wafer pattern dimensions and are the basis for a scaled drawing of the finished
circuit called a composite drawing. During this phase, any constraints, such as
pin configuration, critical speed paths, and any peculiarities of the circuit, are
fed into the CAD system. Modifications to the automatic placement and wire
routing can be manually entered to fulfill any special circuit constraints. These
modifications are automatically checked for layout rule violations.

After all modifications have been made, a computer-driven plotter produces
a symbolic drawing of the circuit. The layout specifies the pattern of each layer
of the integrated circuit. The goal of the layout is to achieve the desired function
of each circuit in the smallest possible space. However, the older method of
drawing circuit layouts by hand (Fig. 2.2) has not been entirely replaced by the
computer. Many parts of a large-scale integrated circuit are still drawn by hand
before being submitted to the computer.

At each stage of this process, including the final stage when the entire
circuit is completed, the layout is checked by means of detailed computer-drawn
plots. Since the individual circuit elements can be as small as a few micrometers across, the checking plots must be greatly magnified. Typically, the plots are 500 times larger than the final size of the circuit.

Figure 2.3 shows the results of a CAD of a complementary MOS (CMOS) ALU bit slice, as an illustrative example. The functional block diagram is shown in Fig. 2.3a. Since the carry section of an ALU often limits its overall performance, the designer may wish to experiment with its circuitry in schematic form, as shown in Fig. 2.3b. Transistors can then be sized and detailed timing simulations performed. Figure 2.3c is a schematic diagram of the ALU showing
Figure 2.2 Hand-drawn composite. (From Ref. 1.)

all transistors. Once the transistor-level circuitry is verified as correct via logic simulation and timing analysis, the layout can be generated (Fig. 2.3d).

The time required to complete the task of circuit design and layout varies greatly with the nature of the circuit. For microprocessors, typically the most difficult circuits to design, the design can take several years and hundreds of engineers. For memories that contain a largely repetitive pattern, the design and layout is accomplished more quickly.

Current LSI or VLSI circuit composite layer drawings may be as much as 20 ft square in size or larger for layout checking and verification purposes (see Fig. 2.4). These drawings are then reduced to the chips' final dimensions using a technique known as digitizing.

When the design and layout of a new circuit is complete, the computer memory contains a list of the exact position of every element in the circuit. From that description in the computer memory a set of plates, called photomasks (see Fig. 2.5), is prepared. Each mask holds the pattern for a single layer of the circuit. Since the circuits are so small, many can be fabricated side by side simultaneously on a single wafer of silicon. Thus each photomask, typically a glass plate about 6–10 in. on a side, has a single pattern repeated many times over its surface.
Figure 2.3  Computer-aided design (CAD) layout example of CMOS ALU bit slice. Beginning with the functional block diagram (a); replacing the carry block with transistor schematics (b); leading to a computer transistor level schematic (c); and culminating in the circuit layout (d).
Figure 2.4  Computer-generated plot of 32-bit microprocessor chip measures 17 ft$^2$. This IC contains 275,000 transistors, which is small by today's standards. (Photograph by Chuck O'Rear, courtesy of Intel Corporation, copyright © 1986.)

MASK MAKING

Generation of the masks is a very detailed process. Typically, it involves generating a complete pattern for each layer of the circuit from the computer memory. This is done by scanning a computer-controlled light spot across a photographic plate in the appropriate pattern.

Figure 2.5  Example of a photo mask. (From Ref. 1.)
This primary pattern, called the *reticle*, is checked for errors and corrected or regenerated until it is perfect. Typically the reticle is 10 times the final size of the circuit. An image of the reticle that is one-tenth its original size is then projected optically on the final mask. The image is reproduced side by side hundreds of times in a process called step-and-repeat. The constraints on both the mechanical system and the photographic system are demanding; each element must be correct in size and position to within less than 0.2 μm. The original plate created by the step-and-repeat camera is copied by direct contact printing to produce a series of submasters. Each submaster serves in turn to produce a large number of replicas, called working plates, that will serve for the actual fabrication process. The working plate may be either a fixed image in an ordinary photographic emulsion or a much more durable pattern etched in a chromium film on a glass substrate. Chrome masks, which are used almost exclusively today, have some distinct advantages over emulsion masks. They last for 15 times as many exposures and they have lower defect levels. A typical mask-making sequence is summarized in Table 2.1.

A complete set of correct masks is the culmination of the design phase in the development of the integrated circuit. Figure 2.6 shows the resultant masks for the 709 operational amplifier of Fig. 2.1. The application sequence of these masks in the fabrication process is shown in Fig. 2.7. The plates are delivered to the wafer fabrication facility, where they will be used to produce the desired sequence of patterns in a physical structure. This manufacturing facility receives silicon wafers, process chemicals, doping materials, and photomasks. Figure 2.8 summarizes the IC design sequence discussed thus far.

The masks, in addition to containing the IC detailed patterns, also have alignment marks and special test sites for process control measurements. Because of the complexity of the circuit patterns, alignment of the masks is very difficult. To simplify this process, alignment guides (or marks) are placed on each mask. These marks can take various shapes, with crosses and squares being the most popular.

Each manufacturing step produces a change in the silicon wafer, which is usually irreversible. If the process is flawed, very expensive scrap is made. The key to control is measurement. Too often variables are in such tiny areas that they cannot be measured, or the measurement is destructive. But if the

### Table 2.1 Typical Mask-Making Sequence

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>1.</td>
<td>Circuit layout</td>
</tr>
<tr>
<td>2.</td>
<td>Digitizing</td>
</tr>
<tr>
<td>3.</td>
<td>Pattern (reticle) generation</td>
</tr>
<tr>
<td>4.</td>
<td>Step and repeat operation</td>
</tr>
<tr>
<td>5.</td>
<td>Generate master plates</td>
</tr>
<tr>
<td>6.</td>
<td>Generate submaster plates</td>
</tr>
<tr>
<td>7.</td>
<td>Generate working plates</td>
</tr>
</tbody>
</table>
measurement is not made and a processing error occurs, the money spent on further wafer processing is wasted.

One solution to this problem is to put a small area for special process control test patterns on each wafer. These patterns range from simple rectangular regions for measuring sheet resistance of diffused layers, or dot patterns for checking alignment of photoresist patterns, to transistor structures typical of those buried deep within an IC. Measurements made on these structures can reveal much about the lot-to-lot reproducibility of processes, and can help pinpoint problems. This information more than compensates for that small area of each wafer that cannot then be used for salable devices.

Figure 2.6 Masks for 709 operational amplifier. (From Ref. 1.)
Figure 2.7 Application of photolithography to produce 709 operational amplifier ICs. (From Ref. 1.)

Figure 2.8 Integrated circuit design flow showing steps from circuit design to photomask generation sequence (From Ref. 2).
IC FABRICATION SEQUENCE

The fabrication of integrated circuits consists of a series or sequence of the following process steps:

- Photolithography
- Dielectric formation
- Doping
- Junction formation
- Silicon deposition
- Metal deposition

Figure 2.9 shows a typical manufacturing sequence using these steps from circuit design to final test for silicon gate (CMOS) technology. More detailed discussions are now presented for each of these processing steps.

One of the major reasons for the use of silicon in fabricating ICs is its ability to grow a natural oxide (silicon dioxide). This oxide layer serves several functions in the manufacturing process.

Surface passivation: A layer of silicon dioxide reduces the susceptibility of the wafer surface to processing contaminates in two ways: It physically prevents the contamination from reaching the silicon, and since the layer grows “down” into the silicon wafer, continually creating a new “surface,” contaminates that may be present on the “old” surface are drawn up into the oxide where they are less dangerous.

Diffusion barrier: During the IC doping process, the dopants actually diffuse (penetrate) into the oxide surface. However, they move more slowly in the oxide than in the silicon. By property selecting the oxide thickness, the dopant is prevented from reaching the wafer surface.

Surface dielectric: At the end of the fabrication sequence the active regions in the wafer are connected by strips of aluminum running along the top of the oxide. The insulating property of the oxide prevents the metallization layer from electrically shorting to the silicon wafer. Shorting can occur if the oxide is too thin and ruptures under a voltage stress, e.g., ESD, or if there are pinholes present in the oxide for any reason. The structure is actually that of a capacitor, with the oxide serving as the dielectric. The region on the device where the oxide serves this function is called the field oxide.

Oxidation

If a wafer of silicon is heated in an atmosphere of oxygen or water vapor, a silicon dioxide film forms on its surface. The film is hard and durable and adheres well. It makes an excellent insulator. The silicon dioxide is particularly important in the fabrication of integrated circuits because it can act as a mask for the selective introduction of dopants.

As a first step in making an IC, the wafer is put in a high-temperature
CONCEPTION OF NEW CIRCUIT: PRELIMINARY SPECIFICATION OF DESIGN ELEMENTS AND FABRICATION PROCESS

COMPUTER-ASSISTED DESIGN AND LAYOUT OF CIRCUIT

GENERATION OF OPTICAL RETICLE

PATTERN GENERATION BY ELECTRON BEAM

MASTER MASKS MADE BY STEP-AND-REPEAT METHOD

Silicon crystal

Oxidation furnace

LPCVD furnace

Mask 1

Plasma etch

Nitrile, oxide removal silicon etch

Implant oxidation

Wafers

Initial oxidation

Deposit silicon nitride

Selective oxidation ("SO") photolithography

Nitride, oxide removal silicon etch

Mask 2

P-well photolithography

Ion implanter

High pressure oxidation furnace

SOMOS thick oxide

Plasma etch

Silicon nitride removal

Diffusion furnace

Drive-in P-well

Chapter 2
Figure 2.9  Typical silicon-gate CMOS manufacture sequence. (Courtesy of ICE Corp.)
Figure 2.9  (Continued)
furnace where an oxide layer is grown over its entire surface. The temperature is usually between 1000°C and 1200°C, and the atmosphere contains oxygen. The exact thickness can be accurately controlled by selecting the appropriate time and temperature of oxidation. For example, a layer of oxide 0.1 μm thick will grow in 1 h at a temperature of 1050°C in an atmosphere of pure oxygen. A layer five times thicker will grow in the same time and at the same temperature in steam.

Forming an oxide layer 10,000 Å thick consumes about 4500 Å of silicon and takes about 4 h to grow. Color changes with thickness, similar to oil film on smooth water, because of changes in the wavelength of reflected light. The color is used to judge the thickness and uniformity of the layer. Oxide layers are sometimes formed by anodizing or, alternatively, by a deposition process. Deposition gives a thick layer without consuming the substrate.

Oxidation and process temperatures are selected out of compromise. The temperature has to be high enough to cause the desired result in an efficient amount of time, but should be as low as is practical to minimize the inducement of crystal defects (this is true for all IC processing steps). At the upper end, 1200°C is the maximum temperature. At 1200°C, wafer warpage becomes excessive (especially for large-sized wafers) and the quartzware starts to sag and has a limited lifetime.

An important aspect of the oxidation process is its low cost. Several hundred wafers can be oxidized simultaneously in a single operation (batch process). The wafers are loaded into slots in a quartz “boat,” separated by only a few millimeters, and the boat is placed in the quartz tube of a furnace similar to a diffusion furnace. The setup of Fig. 2.10 is typical. The high-temperature furnace has a cylindrical heating element surrounding a long quartz tube.

\[ \text{Figure 2.10} \quad \text{Open-tube oxidation-diffusion apparatus. (From Ref. 1.)} \]
purified stream of an oxygen-containing gas passes through the tube. The boats of wafers are loaded into the open end and slowly pushed into the hottest part of the furnace. The temperature in the process zone is controlled to an accuracy of better than one degree. Nitrogen is a protective environment and, in some processes, a carrier gas. Steam for oxidation is obtained by boiling the water in the flask, wet oxygen by bubbling $O_2$ through water heated to about 95°C, and dry oxygen by venting the oxygen tank into the tube directly.

Often the entire oxidation procedure is supervised by a small process control computer that monitors the temperature, directs the insertion and withdrawal of the wafers, and controls the internal environment of the furnace.

**Photolithography**

Fabrication of integrated circuits requires a method for accurately transferring the circuit patterns on each mask to the wafer. The IC is built up layer by layer (see Fig. 2.7), each layer receiving a pattern from a mask prescribed in the circuit design. The photoengraving process known as photolithography, or simply masking, is repeatedly employed for this purpose.

Photolithographic processes are employed in defining all geometries in a device pattern. Lithography involves the patterning of metals, dielectrics, and semiconductors. The patterns can be transferred into a material using either positive or negative masking techniques. The most common patterning technique employed in silicon processing uses a negative-density photomask to produce a positive-density pattern in negative photoresist. (The areas that are desired to be left on a wafer are clear on the photomask.) Ultraviolet (UV) exposure of the negative resist (through the clear areas of the mask) cross-links it, rendering it resistant to the developer-etchant. After development, the undesired material is removed by wet or dry etching where it is not covered by the photoresist.

The difficulties of lithography include resolution and etchability. While acceptable resolution may be achieved in most fabrication steps, the most critical gate processing in field effect transistor fabrication requires less than 0.5-µm resolution for state-of-the-art devices. In addition, some layers that must be patterned are not easily etched or may have poor selectivity compared to masking materials. Wet etchants usually achieve poorer resolution than plasma-etching techniques.

Most IC processes require a set of 5–10 such patterns, sometimes more. Each pattern must be aligned precisely with those already on the wafer. In making complex ICs, patterns must be aligned to within typically less than 0.2 µm across the entire area of a 200-mm (8-in.) wafer, for example. The difficulty is that line widths of 0.5 µm are commonly used in making ICs. A complex IC contains thousands of these 0.5-µm lines. So the patterns in all masks must align with each other to within substantially less than 0.5 µm. Without accurate mask alignment, yield drops rapidly to zero.
For first mask alignment there is no pattern on the wafer to align to. The pattern has to be aligned to the crystal structure of the wafer. Since the crystal structure is not visible, the alignment operator aligns the mask pattern to the major wafer flat (Fig. 2.11). This is why all of the patterns are at right angles to the flat.

With manual alignment systems, the wafer flat is positioned on the aligner stage to an accuracy of ±2 degrees. On automatic aligners this step is automatically controlled.

After alignment to the flat, the wafer is automatically positioned under the mask and the exposure subsystem activated. First mask alignment requires no operator attention after the flat is positioned, and is the least critical in the entire process. All subsequent masks are aligned to patterns existing on the wafer via alignment marks in an automated alignment system.

It should be noted that within a mask set, two or three of the masks are more critical than the others. Also, within a particular mask level there are usually parts of the circuit that are more alignment sensitive than others.

A method of mask alignment and exposure used through the 1970s was called contact printing. In this method (which was useful through MSI device complexity) the mask is held just off the wafer surface and is visually aligned with the patterns in the wafer. The machine holding the wafer and mask for this operation can be adjusted to an accuracy of 1–2 μm. After alignment is achieved, the mask is pressed into contact with the wafer and then impinged with ultraviolet radiation to expose the photoresist. The space between the wafer and the mask is often evacuated to achieve intimate contact; atmospheric pressure squeezes the

![Figure 2.11](image_url) First mask align. (From Ref. 2.)
wafer and the mask together. In another variation, proximity printing, the mask is held slightly above the wafer during exposure.

Variations in the masking process arise from the need to print very small features with no defects in the pattern. If the mask were to be positioned very far from the surface, diffraction of the ultraviolet radiation passing through the mask would cause the smaller features to blur together. Thus hard contact would be preferred. However, the use of contact printing resulted in a number of yield and production problems, all due to the constant physical contact of the mask and the photoresist layer: damage to both mask and photoresist layer, poor dimensional control, and short mask life.

This brought about the projection alignment and exposure system, in which the mask and wafer never touch. Using projection alignment, the image of the mask is projected onto the wafer through an optical system. In this case mask life is virtually unlimited since there is no mask or photoresist damage. Projection alignment has become the standard production method for LSI and VLSI devices.

The concurrent increase in wafer size and decrease in device geometries presents a continuing problem in designing optics capable of forwarding an accurate image over the larger area. A replacement method for projection alignment currently being used for state-of-the-art ICs is called direct write.

The basic photoresist process (Table 2.2) may vary considerably from IC supplier to supplier, depending on the type of photoresist used, device features, and proprietary considerations. The photolithographic-photoresist processing steps are pictorially depicted in Fig. 2.12. The numbers in the following discussion refer to the respective steps shown in the figure. To form a doped pattern (which is contained on a mask) in the wafer by diffusion or implantation, openings must first be made in the oxide layer. The most basic masking step

<table>
<thead>
<tr>
<th>Table 2.2 Basic Photoresist Process Steps</th>
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</thead>
<tbody>
<tr>
<td>1. Substrate preparation: oxidation, CVD</td>
</tr>
<tr>
<td>2. Surface preparation: clean, dehydrate, prime</td>
</tr>
<tr>
<td>3. Application of resist: spin, spray, roll, dip</td>
</tr>
<tr>
<td>4. Soft bake: low-temperature cure to dry resist</td>
</tr>
<tr>
<td>5. Expose: align and expose to selectively polymerize the resist</td>
</tr>
<tr>
<td>6. Develop: dissolve the unpolymerized resist</td>
</tr>
<tr>
<td>7. Visual inspection (develop check): verify accurate image transfer to the photoresist</td>
</tr>
<tr>
<td>8. Hard bake: higher temperature cure to completely dry and polymerize the resist</td>
</tr>
<tr>
<td>9. Strip resist: organic, asher, or acid removal of resist</td>
</tr>
<tr>
<td>10. Etch: oxide</td>
</tr>
<tr>
<td>11. Visual inspection (final inspection): verify accurate image transfer to the layer</td>
</tr>
</tbody>
</table>
involves the etching of a pattern into an oxide. An oxidized wafer (1) is first coated with photoresist, a light-sensitive polymeric material (2). Photoresist may be applied to the wafer by many different techniques, including dipping, brushing, spraying, or roller coating. The most popular, however, is the use of a spinner to apply the solution (photoresist dissolved in a solvent).
In spinning, a wafer is held in place by vacuum on a wafer holder. Resist is then dispensed onto the center of the wafer, which starts to spin. The physics involved in the process force the resist toward the edges of the wafer, while providing a uniform coat of solution. The excess is spun off the wafer. As the liquid film (coat) spreads over the surface, the solvent evaporates, leaving the polymeric film. A mild treatment is given to dry out the film thoroughly and to enhance its adhesion to the silicon dioxide layer under it.

A combination of spin speed and the viscosity of the resist is responsible for the thickness of the resist following its application. Each resist has different specified high and low spin speeds for maximum uniformity. If the spin speed is too low, an excessive edge beam will form; if too high, a nonuniform layer will result because of uneven evaporation of the solvent in the resist. Although the process appears to be a simple one, it is nonetheless fraught with the possibility of contamination.

The most important property of the photoresist is that its solubility in certain solvents is greatly affected by exposure to ultraviolet radiation. For example, a negative photoresist cross-links and polymerizes wherever it is exposed. Thus exposure through a mask followed by development (washing in the selective solvent) results in the removal of the film wherever the mask was opaque. The photoresist pattern is further hardened after development by heating.

The photoresist-coated wafer is exposed to ultraviolet light (3) through the appropriate photomask pattern to expose areas of the resist. Two methods receiving attention as possible replacements for ultraviolet exposure in the future are X-ray and electron-beam (e-beam) exposure. The exposure renders the photoresist soluble in a development solution (4). Next, the wafer with its photoresist pattern is placed in a solution of hydrofluoric acid. The acid dissolves (etches) the oxide layer wherever it is unprotected, but it does not attack either the photoresist or the silicon wafer itself (5). After the acid has removed all the silicon dioxide from the exposed areas the wafer is rinsed and dried, and the photoresist pattern is removed by another chemical treatment (6).

The etching operation serves a dual purpose: to remove portions of the top layer of the wafer through the holes, or openings, in the photoresist layer; and to transfer the pattern with those dimensions into the top layer of the wafer. The etch operation must not disturb the underlaying wafer surface. Etching down into the underlying layer can drastically change the physical dimensions as well as electrical and functional characteristics of the device—even to the point of catastrophic failure.

Other films are patterned similarly. For example, a warm solution of phosphoric acid selectively attacks aluminum and therefore can serve to pattern an aluminum film. Often an intermediate masking layer is needed when the photoresist cannot stand up to the attack of some particular etching solution. For
example, polycrystalline silicon films are often etched in a particularly corrosive mixture containing nitric acid and hydrofluoric acid. In this case, a film of silicon dioxide is first grown on the polycrystalline silicon. The silicon dioxide is patterned in the standard fashion and the photoresist is removed. The pattern in the silicon dioxide can now serve as a mask for etching the silicon film under it, since the oxide is attacked only very slowly by the acid mixture.

The regions now free of oxide can be accessed by diffusion or implantation to add dopants to these areas.

**Doping**

Dopant elements may be added to the silicon at several points in the IC manufacturing process. Principal compounds used for doping silicon are listed in Table 2.3.

There are two techniques for selectively introducing dopants into the silicon crystal: diffusion and ion implantation.

**Diffusion**

Diffusion is a naturally occurring time- and temperature-dependent process used in IC production that introduces small amounts of impurities into the silicon substrate material and permits the impurity to spread into the substrate after the photomasking sequence has taken place (i.e., after the open areas are made in the oxide coating and the photoresist is removed).

If silicon is heated to a high temperature, say 1000°C, the impurity atoms

<table>
<thead>
<tr>
<th>Element</th>
<th>Dopant type</th>
<th>Compound</th>
<th>Formula</th>
<th>Normal state</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antimony</td>
<td>n</td>
<td>Antimony trioxide</td>
<td>Sb₂O₃</td>
<td>Solid</td>
</tr>
<tr>
<td>Arsenic</td>
<td>n</td>
<td>Arsenic trioxide</td>
<td>As₂O₃</td>
<td>Solid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Arsine</td>
<td>AsH₃</td>
<td>Gas</td>
</tr>
<tr>
<td>Phosphorus</td>
<td>n</td>
<td>Phosphorus pentoxide</td>
<td>P₂O₅</td>
<td>Solid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Phosphorus oxychloride</td>
<td>POCl₃</td>
<td>Liquid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Phosphorus tribromide</td>
<td>PBr₃</td>
<td>Liquid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Phosphine</td>
<td>PH₃</td>
<td>Gas</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Silicon pyrophosphate</td>
<td>SiP₂O₇</td>
<td>Solid</td>
</tr>
<tr>
<td>Boron</td>
<td>p</td>
<td>Boron trioxide</td>
<td>B₂O₃</td>
<td>Solid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Boron tribromide</td>
<td>BBr₃</td>
<td>Liquid</td>
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<tr>
<td></td>
<td></td>
<td>Diborane</td>
<td>B₂H₆</td>
<td>Gas</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Boron trichloride</td>
<td>BCl₃</td>
<td>Gas</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Boron nitride</td>
<td>BN</td>
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</tbody>
</table>
begin to move slowly through the crystal. Certain key impurities (boron and phosphorus) move much more slowly through silicon dioxide than they do through silicon itself. This important fact enables one to employ thin oxide patterns as impurity masks. For example, a boat of wafers can be placed in a furnace at 1000°C in an atmosphere containing phosphorus. The phosphorus enters the silicon wherever it is unprotected, diffusing slowly into the bulk of the wafer. After enough impurity atoms have accumulated, the wafers are removed from the furnace, and solid-state diffusion effectively ceases. Of course, every time the wafer is reheated the impurities again begin to diffuse; hence all planned heat treatments must be considered in designing a process to achieve a specific depth of diffusion. The important variables controlling the depth to which impurities diffuse are time and temperature. For example, a layer of phosphorus 1 μm deep can be diffused in about an hour at 1100°C. Diffusion times range from a few seconds to many hours, depending on the desired depth of the diffused layer to be produced.

To achieve maximum control, most diffusions are performed in two steps. The predeposition, or first step, takes place at a furnace temperature selected to achieve the best control of the amount of impurity introduced. The temperature determines the solubility of the dopant in the silicon, just as the temperature of warm water determines the solubility of an impurity such as salt. After a comparatively short predeposition treatment the wafer is placed in a second furnace, usually at a higher temperature. This second heat treatment, the "diffusion drive-in" step, is selected to achieve the desired depth of diffusion.

**Predeposition**

To dope a semiconductor wafer, the appropriate atoms must first be made available on the surface of the wafer. Several methods are available for this purpose. An appropriate compound of the desired element in the form of a solution of controlled viscosity can be "painted" on the surface of the wafer, or spun on in the same manner in which photoresist is normally applied. For spin-on dopants, viscosity and spin rate are controlled to achieve the desired dopant film thickness. After evaporation of the solvent, the wafer is normally subjected to a selected high temperature to complete the predeposition diffusion. Excess dopant is then removed (usually by etching) prior to dopant drive-in.

Another method of predeposition employs a low-temperature chemical vapor deposition (CVD) process to deposit an oxide of the desired element on the wafer. In this case, the dopant is introduced as a gaseous compound—usually in the presence of nitrogen (or other inert gas) as a "carrier" or diluent, and generally with an excess of oxygen present to ensure deposition of the dopant as an oxide. Typically used gases are arsine, phosphine, diborane, and boron trichloride. In this operation, the oxygen concentration must be carefully controlled, since the presence of too much oxygen can lead to oxidation of the
silicon surface of the wafer, in which case the silicon dioxide formed would block entry of the dopant.

Yet another method employs a doped layer of silicon dioxide in contact with the surface of the wafer. Inasmuch as the solid solubility of dopant is greater in silicon than in silicon dioxide, at elevated temperature the dopant will migrate from the SiO$_2$ into the silicon.

Following this predeposition operation, the concentration of dopant at the surface of the wafer will be that determined by the temperature and solid-solubility relationship, decreasing with depth beneath the surface. The depth of penetration and the amount of predeposition diffusion will be a function of both predeposition time and temperature. Dopant is usually introduced only at selected locations on the wafer surface by means of an appropriate mask (often silicon dioxide), which blocks or inhibits introduction of the dopant wherever it is present.

**Diffusion Drive-In**

Following dopant predeposition, a dopant wafer is subjected to a (different) elevated temperature, during which the dopant atoms further diffuse into the silicon crystal lattice. The rate at which they diffuse, or are “driven” into the wafer, can be controlled by the specific temperature employed. As diffusion progresses, the concentration of dopant, which remains greatest at the point of dopant introduction—the wafer surface—decreases as the dopant atoms migrate further into the crystal lattice. The dopant atoms migrate further into the crystal lattice. The dopant profile for a specific purpose is thus achieved by control of the diffusion step. Dopant drive-in is usually performed in an oxidizing atmosphere to regrow a protective layer of silicon dioxide over the newly diffused area.

In the formation of p-n junctions by solid-state diffusion, the impurities diffuse laterally under the oxide mask about the same distance as the depth of the junction. The edge of the p-n junction is therefore protected by a layer of silicon dioxide. This is an important feature of the technique, because silicon dioxide is a nearly ideal insulator, and many electronic devices will not tolerate any leakage at the edge of the junction.

**Ion Implantation**

Until the early 1970s diffusion was the primary doping procedure used in IC fabrication. However, the increased use of MOS devices and smaller geometries pointed to several deficiencies or limiting features of the diffusion process:

1. Diffusion cannot provide the control required for low-concentration doping of the gate region of MOS devices.
2. Diffusion creates a higher concentration of the dopant at the wafer
surface. What does this mean? Since current travels where the dopants are concentrated during device operation, any surface contamination severely affects an MOS device’s operation.

3. The side diffusion (Fig. 2.13) inherent in the diffusion process limits how closely individual on-chip devices can be placed next to each other, creating larger chip size, slower speed, and lower yield circuits.

4. Each high-temperature heat treatment required for diffusion affects yield in two ways: (1) it causes some crystal damage in the wafer and (2) it diffuses unwanted contaminants into the wafer.

The ion implantation process was developed to overcome these deficiencies. Additionally, ion implantation (1) provides the ability to dope the wafer through a thin oxide layer and (2) allows the use of photoresist and other layers as the doping mask. The ion implantation process, which does not occur naturally, uses high-voltage ion bombardment of selected impurities into controlled and selected regions of the wafer at room temperature to achieve the desired device operating characteristics without any intervening chemical reaction or diffusion. In this process, a compound of the desired element is ionized (stripped of one or more of its electrons) in the gaseous state. The desired ions are then separated from all other ions present by deflecting them through a magnetic field—in much the same manner as a mass spectrometer uses to separate materials on the basis of their charge-to-mass ratio.

The separated ions are accelerated to a high energy by passing them through a potential difference of tens of thousands of volts and focused onto the surface of the wafer, which they penetrate to a depth that depends upon their mass and kinetic energy. They can thus be implanted at selected depths within the wafer. The wafer can be selectively masked against the ions either by a patterned oxide layer, as in conventional diffusion, or by a photoresist pattern. For example, phosphorus ions accelerated through a potential of 100,000 V will penetrate the photoresist to a depth of less than half a micrometer. Wherever they strike bare silicon they penetrate to an average depth of a tenth of a micrometer. Thus even a 1-μm layer of photoresist can serve as a mask for the selective implantation of phosphorus.

![Figure 2.13](image) Side diffusion. (From Ref. 2.)
As the accelerated ions plow their way into the silicon crystal they cause considerable damage to the crystal lattice. It is possible to heal most of the damage, however, by annealing the crystal at a moderate temperature. Little diffusion takes place at the annealing temperature, so that the ion implantation conditions can be chosen to obtain the desired distribution. For example, a very shallow, high concentration of dopant can be conveniently achieved by ion implantation. A more significant feature of the technique is accurately controlling the concentration of the dopant. The ions bombarding the crystal each carry a charge, and by measuring the total charge that accumulates the number of impurities can be precisely determined. Hence ion implantation is used whenever the doping level must be very accurately controlled. Often ion implantation simply replaces the predeposit step of a diffusion process. Ion implantation is also used to introduce impurities that are difficult to predeposit from a high-temperature vapor. For example, the use of arsenic as a shallow n-type dopant in MOS devices coincides with the availability of suitable ion implantation equipment.

A unique feature of ion implantation is its ability to introduce impurities through a thin oxide. This technique is particularly advantageous in adjusting the threshold voltage of MOS transistors. Either n-type or p-type dopants can be implanted through the gate oxide, resulting in either a decrease or an increase in the threshold voltage of the device. Thus by means of ion implantation it is possible to fabricate several different types of MOS transistors on the same wafer.

While ion implantation is more precise than photomasking, wafers can be processed only one at a time, rather than in large batches. Nonetheless, as device design moves increasingly toward smaller, shallower, and lower concentration dopings, better doping control, and more doped layers per process, ion implantation will become the dominant doping technique. Diffusion will still find a use in the doping of the less critical layers and will continue to be the preferred doping method for lower integration level circuits. Figure 2.14 shows a carousel of wafers awaiting ion implantation.

For all ICs the oxidation, photomasking, and diffusion or implantation sequence must be repeated several times to create the desired device structure.

Table 2.4 summarizes the salient features of the ion implantation process step just discussed, while Table 2.5 highlights the various ion implantation methods currently being used.

DEPOSITING LAYERS ON THE WAFER SURFACE

The uppermost layers of integrated circuits are formed by depositing and patterning thin films on the surface of the wafer. These layers can be dielectrics, semiconductors, or conductors and are placed on the wafer by a variety of
Figure 2.14 Technician prepares a carousel of gallium arsenide wafers for insertion into ion implantation system. (Courtesy of Sanders, division of Lockheed Aircraft Corp.)
Table 2.4  Ion Implantation

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Good overall doping accuracy</td>
<td>Complex equipment required</td>
</tr>
<tr>
<td>Unaffected by surface films</td>
<td>Slow for heavy doses</td>
</tr>
<tr>
<td>Low temperature process</td>
<td>Wafer heating limits ion rate</td>
</tr>
<tr>
<td>Can mask patterns if desired</td>
<td>May need diffusion step</td>
</tr>
<tr>
<td>Can implant deep layers, including</td>
<td>Possible bombardment damage</td>
</tr>
<tr>
<td>dielectrics</td>
<td>Scanning may cause local doping</td>
</tr>
<tr>
<td>Can implant dopants through thin oxide layer; useful for adjusting threshold voltage of MOS transistors</td>
<td>Not a batch process</td>
</tr>
</tbody>
</table>

techniques. The use of these thin films is critical in providing the desired levels of performance in LSI and VLSI circuits. In fact, because the fabrication of LSI and VLSI circuits contains more thin film steps than diffusion steps, these circuits are essentially film technology driven. This represents a significant departure from the diffusion-driven fabrication of SSI and MSI circuits. Therefore thin-film technology is probably more critical to the overall yield and performance of these circuits than are the diffusion and oxidation steps.

Thin-film layers are used at places in the fabrication process where rapid low-temperature growth is essential. One such use is the selection of areas on the wafer that are to be oxidized. This is because silicon nitride oxidizes much more slowly than does silicon. Thus, a layer of silicon nitride can be vapor

Table 2.5  Ion Implantation Methods

<table>
<thead>
<tr>
<th>Low/medium current</th>
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<tbody>
<tr>
<td>Serial, electrically scan ion beam across wafer</td>
</tr>
<tr>
<td>One wafer at a time, very slow for higher doses</td>
</tr>
<tr>
<td>Most useful for low doses</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>High current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Batch, wafers repeatedly moved under beam</td>
</tr>
<tr>
<td>Used for higher doses and/or throughout</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>High energy (very high voltage)</th>
</tr>
</thead>
<tbody>
<tr>
<td>For deeper dopant penetration</td>
</tr>
<tr>
<td>Can produce buried dielectric layer</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Focused ion beam</th>
</tr>
</thead>
<tbody>
<tr>
<td>Implantation writing, eliminates lithography</td>
</tr>
<tr>
<td>Serial, very slow</td>
</tr>
</tbody>
</table>
deposited, patterned, and used as a oxidation mask. The resulting surface is much flatter than would be the case if the thick oxide were grown everywhere and selectively removed. For n-channel MOS devices there is the additional advantage that an ion implantation step involving boron can be added just before the oxidation step, relying on the nitride pattern as a mask. This procedure results in a heavily doped p-type region located precisely under the oxide, which acts as an obstacle to the formation of channels from adjacent elements in the device.

This "channel stopper" diffusion step is necessary in high-performance n-channel MOS technology. Without selective oxidation a special masking step would have to be added. The spacing between elements would then necessarily be larger; thus selective oxidation leads to greater circuit density. Bipolar integrated circuits also benefit greatly from the use of selective oxidation. By replacing the conventional diffused isolation with oxide isolation the space taken up by one bipolar transistor is reduced by more than a factor of four.

Another use of thin film is for the planarization of the wafer surface. The starting material for an IC is essentially flat. However, the process of photolithographic patterning, combined with the growth or deposition of both insulating and conducting films, results in an increasingly nonplanar structure as the wafer proceeds through all fabrication steps to the metallization stage. Typically, the gate oxide of a MOS transistor may be 90–200 Å thick, whereas the thickness of a neighboring field oxide may be as much as 3,000–7,000 Å. This presents a severe problem in maintaining step coverage of metallization patterns, often resulting in a break in continuity at the step.

Step coverage refers to how well the interconnection material will adhere to the nearly vertical sides of the contact holes in the insulting oxide that reach down to the previous connecting layer. The more vertical the edges, the more likely the interconnection material will have a problem adhering to the inside and outside corners of the contact-hole step. Ideally, suppliers would like the height of that step to be zero, but this is not possible since an insulator is needed in most cases. This problem is especially serious in VLSI circuits, where the lateral dimensions are reduced but the metallization and oxide thicknesses are relatively unchanged. In these applications, techniques for flattening these steps, commonly referred to as planarization, greatly improve the process yield.

One solution is to thin the oxide without increasing the possibilities of punchthrough or pinholes that would cause catastrophic circuit failure by using nitride layers.

The local oxidation step itself results in considerable planarization, especially if the silicon is pre-etched so that the final oxide is fully recessed. Other approaches are aimed at removing the abrupt step when a cut is made in the oxide by taper control means using material such as PSG and polymide with such techniques as ion implantation damage and plasma etching.
The list that follows summarizes the uses for thin films:

1. Thick field oxides for MOS ICs as well as for high-voltage devices. These are usually deposited over a base layer of thermally grown oxide to avoid a high trap density at the silicon surface.
2. Films where the previously grown layer has been removed—for example, deep diffusions of the type used for buried layers and isolation wells. These often utilize fresh masking and redoping at some point during the diffusion process.
3. Insulating layers over a metallization layer to form a base for the next layer of metal.
4. Planarization of wafer surface.
5. Passivation layers to protect the IC from physical abuse during mounting and packaging.

Traditionally, physical vapor deposition (PVD) techniques (i.e., evaporation and sputtering) have been used to deposit aluminum, alloys of aluminum, and a variety of silicides. The problems encountered with PVD, however, include the incorporation of oxygen and carbon in the deposited films, poor step coverage (which is marginal with evaporated films), and films with poor composition control, large volume shrinkage, and high stress. Although cosputtering from individual targets of a refractory metal and silicon improves composition control, other film properties are still difficult to control.

Chemical vapor deposition (CVD) can produce pure, reproducible thin films with good composition control. CVD films have lower stresses and, generally, have conformal step coverage.

The predominant methods for depositing thin films are

1. Oxidation (discussed earlier)
2. Epitaxy
3. Chemical vapor deposition
4. Evaporation
5. Sputtering

Each of the latter four are now discussed.

**Use of Dielectric Layers***

When used in insulating applications in multilevel VLSI circuits, dielectric films must possess the following attributes:

*Portions of this section used with permission from Ref. 3.
Chapter 2

Must sustain relatively high dielectric breakdown fields
Should have a low dielectric constant, to minimize parasitic capacitance between conductors, and a high electrical resistivity
Must have a low loss factor for high-frequency applications
Must be free of pinholes and microcracks
Should have low compressive stress and excellent adhesion properties
Must allow hydrogen to diffuse through them during annealing to remove the interface states
Must be able to getter or to block alkali ions

For VLSI circuits all dielectric films must be readily depositable at temperatures compatible with other device structural materials and device performance requirements. Deposition must be done with excellent compositional control and good step coverage. In some cases the films must be flowed thermally for contour tapering or planarization. Finally, dielectric films must be patternable by precision lithography and selective etching.

Table 2.6 lists the major uses for dielectric films in the fabrication of VLSI circuits. Some of these will be discussed in greater detail.

Vertical insulation of conductor levels may be considered the most important application of deposited dielectrics in advanced multilevel VLSI devices. In addition to providing defect-free electrical insulation between layers, deposited dielectric films must ensure the continuity and uniformity of subsequently deposited conductor films that are frequently deposited over steep topography.

For high-temperature insulation, this is usually accomplished by fusion tapering or planarization of a glass, typically CVD phosphosilicate glass (PSG). The high temperature (1000–1100°C) required to soften PSG is undesirable and, for many ICs, intolerable. This is especially true in the fabrication of advanced devices with short channel lengths and shallow junctions where lateral and vertical diffusion of dopants must be minimized. Also, devices that must resist high levels of radiation require processing temperatures substantially lower than those acceptable for commercial IC production.

Lower process temperatures are also desirable to avoid the generation of crystallographic defects and wafer warpage, and to avoid the diffusion of contaminants.

Fusion tapering of silicate glasses solves the problems of metal coverage in most device applications. However, for high-density multilevel VLSI devices with the most stringent demands on precision lithography, creation of a nearly planar surface may offer certain advantages, such as improved metal definition, step coverage, and linewidth control.

The processing of interlevel insulation for aluminum and alloy conductors at the upper levels of device structures must be kept at temperatures not exceeding