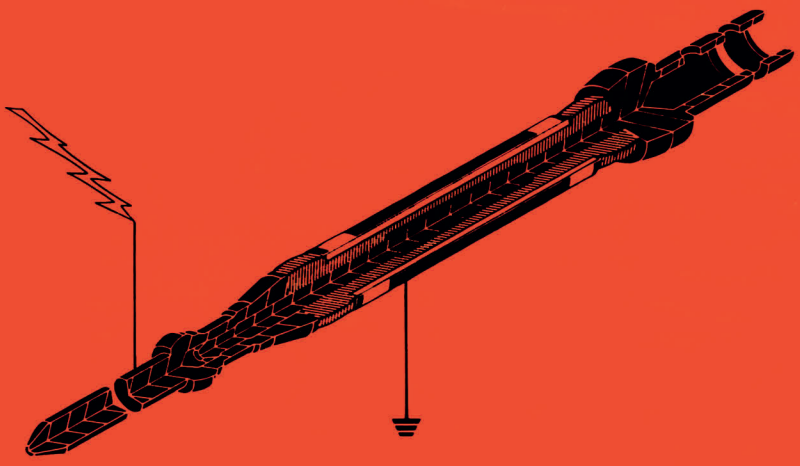
Electronic Ceramics

Properties, Devices, and Applications



edited by
Lionel M. Levinson

Electronic Ceramics

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A Series of Reference Books and Textbooks

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edited by **Lionel M. Levinson**

General Electric Company
Schenectady, New York

MARCEL DEKKER, INC. New York and Basel

Library of Congress Cataloging-in-Publication Data

Electronic ceramics.

1. Electronic ceramics. I. Levinson, Lionel M.
TK7871.15.C4E418 1987 621.381 87-20120
ISBN 0-8247-7761-1

MARCEL DEKKER, INC.
270 Madison Avenue, New York, New York 10016

Current printing (last digit):
10 9 8 7 6 5 4 3 2

PRINTED IN THE UNITED STATES OF AMERICA

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Preface

High technology ceramics are an essential part of the electronic and electrical equipment used for consumer, industrial, and military applications and electronic ceramics are integral components of the circuits used in computers, signal processing, telecommunications, power transmission, and power control technologies. These materials play a ubiquitous but often little-noticed role in our daily lives.

Historically, the invention of the transistor in 1948 initiated a surge of development in electronic devices. Germanium and later silicon and gallium arsenide semiconductor devices were prepared from very high purity single crystals of unparalleled perfection. Today the drive toward large-scale integrated circuits continues to fuel a massive research and development effort in single-crystal semiconductor materials and circuits.

In contrast, the development of electronic ceramics has undergone a slower evolutionary growth. The vast majority of polycrystalline ceramics are produced using less-defined synthesis and manufacturing processes, and progress in the field is often made with a judicious mix of scientific inspiration, Edisonian perspiration, and educated ingenuity. In addition, these materials can possess significant macroscopic and microscopic defects. Uncontrolled impurity levels easily exceed 100 ppm--orders of magnitude greater than that typical in crystalline semiconductors. The ceramic grains and grain boundaries determining ceramic device behavior are internal to the material and generally irregular, not easily accessible or subject to independent control. These difficulties have impeded electronic ceramic materials research and device design and fabrication.

These problems notwithstanding, many significant developments have occurred in electronic ceramics technology. Noteworthy are

Japanese and Dutch ferrite research (1935-1950); titania and ferroelectric research and development in the United States (1940-1960); Japanese-U.S. alumina developments for thick-film microelectronics (1950-1970); activities on nonlinear conduction and semiconduction in oxide ceramics in Europe, the United States, and Japan (1940-1980); and recent Japanese advances in ceramics with high thermal conductivity for integrated circuit packaging (1980-present).

In the last few months the scientific community (and indeed science as a whole) has been electrified by the discovery of high-temperature oxide ceramic superconductors. Superconductivity at temperatures in excess of liquid nitrogen (77°K) was demonstrated early in 1987 in perovskite compounds of the type $YBa_2Cu_3O_{7+X}$. These superconducting ceramics have rapidly been produced as evaporated and sputtered thin films, sintered and plasma-sprayed thick films, single crystals, and shaped ceramics. An intense, worldwide effort involving thousands of scientists and engineers is currently underway to understand the properties of these materials and produce them in technologically useful forms and with useful device structures. Many questions remain unresolved as this book goes to press: critical currents are very low, the role of grain boundaries is unclear, and the basic forces producing high temperature superconductivity are not understood. In spite of the present uncertainties, we may, however, venture to predict that high-temperature ceramic superconductors will have an impact of some significance on modern technology. Certainly the size of the effort and the enthusiasm of the workers in the field is unprecedented in recent times.

The material presented in this book is addressed to those scientists and engineers who need to use a particular electronic ceramic device or material in their specific application. While each chapter is relatively self-contained and provides adequate introductory materials, the emphasis is on the properties and configuration of the ceramic which facilitates proper application of material to the task at hand. Accordingly, this book is intended for workers in the fields of electronics, ceramics, computers or telecommunications, and so on, to broaden their expertise in the area of electronic ceramics. The various book chapters are authored by experts in the field and treat integrated circuit packaging, piezoelectric devices, magnetic ceramics, surge protection devices, thick film technology, optical and electro-optical ceramics, and high-temperature oxide superconductors. The references and tabular and graphical materials are up to date and sufficiently complete to provide a valuable reference text for practicing electronic engineers and ceramists, as well as for graduate students in materials science, electrical engineering,

or ceramic technology. It is hoped that the material contained in this volume will contribute to an increased awareness and recognition of the role played by electronic ceramics in the technological structure of the twentieth century.

Lionel M. Levinson

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1

Ceramic Packaging of Integrated Circuits

BERNARD SCHWARTZ *IBM Corporation, T. J. Watson Research Center, New York*

1.1 INTRODUCTION

The packaging of integrated circuits requires a knowledge of ceramics and metals to accommodate the fabrication of modules that are used to construct subsystems and entire systems from extremely small components. The electronic component is the smallest replaceable element in the system.

The use of ceramics in electronic packaging has advanced to the very sophisticated levels of science and engineering. The first applications were to substrates, which were needed to start the emerging microelectronics era. These technologies were used to create the next generation of packages. New materials and processes had to be developed to build these ceramic modules. The first substrates were made with steatite ceramics, which were sintered in air at temperatures in the range of 1200-1350°C. These substrates were metallized with various pastes, such as gold, silver, palladium, and platinum. The steatite ceramics were soon replaced with alumina materials and were metallized with Mo, W, and Mo-Mn pastes. The latter three pastes had to be sintered in reducing atmospheres. Eventually, the alumina ceramics could be cofired with these pastes.

Early packaging of single diode and transistor devices consisted of producing hermetic seals and electrical connections with adequate provisions for mounting and power distribution. Microelectronics has brought together many circuits into a single chip and many chips into a single package. The functions of these packages are reviewed later in this chapter, and the next section discusses the history of ceramics as they are used to package integrated circuits.

1.2 HISTORY

Originally, ceramic-metal packages were used for interconnections and environmental protection of diodes and transistors. Since the inception of these packages, the number of applications has grown to such an extent that they are now also utilized for intraconnections, substrates, power distribution, cooling, inputs, outputs, and engineering changes. In the future, growth of the electronics industry will place new and even more demanding requirements for improved materials and processes. These needs will probably be greatest in the computer field, where the cost per computation will have to be reduced to handle the large amounts of data and their manipulation in the central processor (Schwartz, 1969, 1984a, b).

The sequential development and use of component interconnections are shown in Fig. 1;

Wires, metal chassis, and sockets (Fig. 1A)
Epoxy-glass printed circuit boards, connectors, and cables (Fig. 1B)
Modules, cards, and multilayer boards (Fig. 1C)
Multilayer modules and multilayer boards (not shown)

The history of the microelectronics era is summarized in Fig. 2. Radio tubes were the first devices to use glass-metal seals. The next ceramic application, a proximity fuse, was used to explode shells upon impact during World War II. This device consisted of a ceramic substrate upon which screened resistors, conductors, and capacitors were either fired or attached.

In the mid-1950s to early 1960, Project Tinkertoy was initiated, which utilized steatite substrates for the mounting of resistors, capacitors, conductors, and vacuum tubes. Riser wires were used to make the connections between substrates. These ceramic substrates were produced in several ceramic manufacturing plants, such as that of the American Lava Corporation. This project was short-lived because of the introduction of semiconductor devices.

The microelectronics era began in earnest in 1955 with the development of diodes and transistors. These devices had to be hermetically sealed to avoid contamination from moisture and impurities, which could affect their performance. In Fig. 3, the first glass-metal sealed headers for diodes and transistors are shown. The early ceramic flat packs are depicted in Fig. 4, which were also used to package diodes and transistors.

In 1958, the U.S. Army Signal Corps and the RCA Corporation launched the Micromodule Project in an attempt to miniaturize battlefield communications equipment, such as helmet radios. The substrate elements used in these modules are shown in Fig. 5A, an assembled

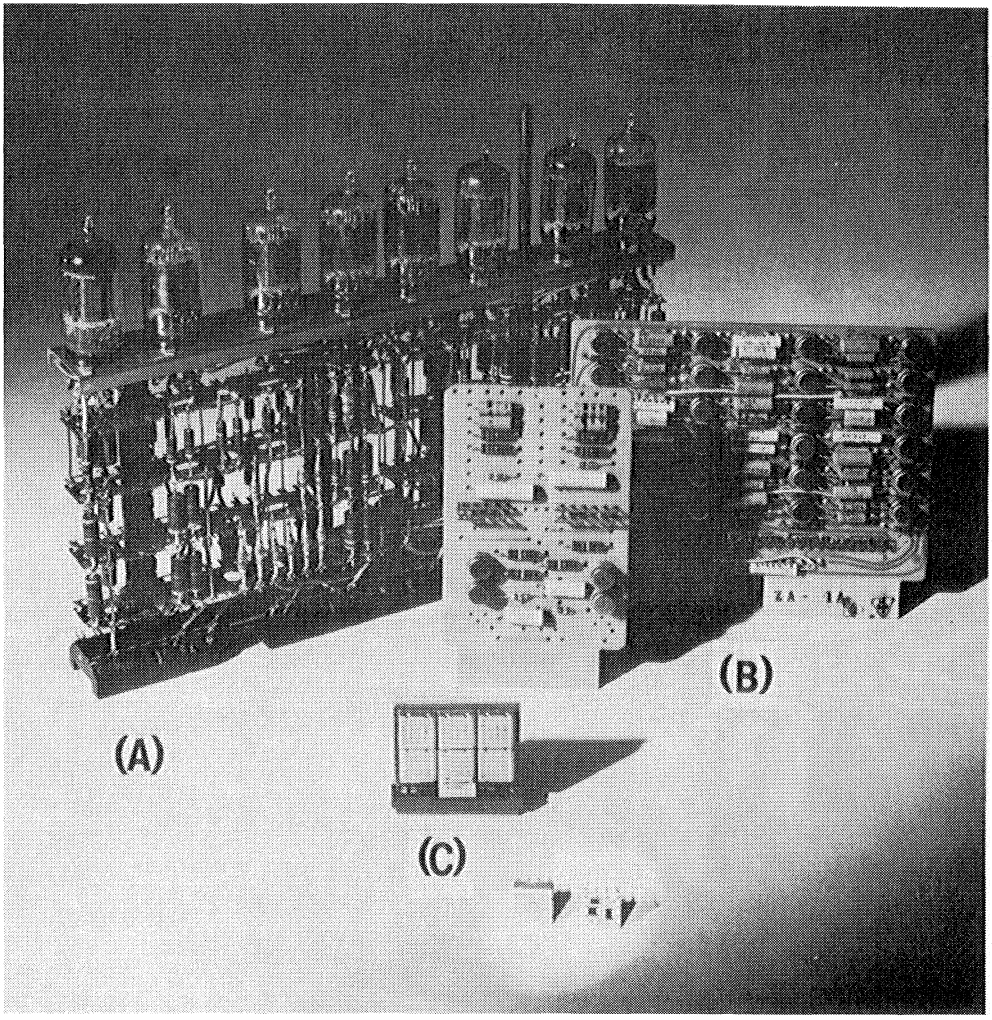


FIGURE 1 Packaging systems: (A) Wires, metal chassis and sockets, (B) epoxy-glass printed circuit boards, connectors and cables, (C) modules, cards and multilayer boards.

module in Fig. 5B, and an encapsulated module in Fig. 5C. These modules attempted to use a common substrate form factor, which was 0.3 by 0.3 in. and 0.01 in. or greater in thickness and had three notches on each edge in order to solder the riser wires to the perimeter of each wafer. These substrates were composed of either a 96%

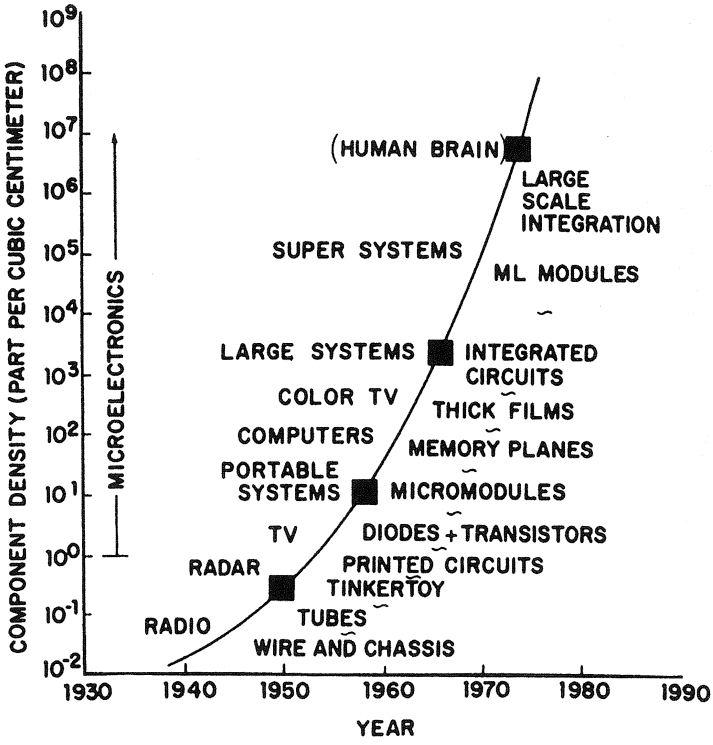


FIGURE 2 History of microelectronics, showing the relationship between component density and year of technology.

alumina ceramic or other various titanate dielectrics (Schwartz and Stetson, 1960).

This project succeeded in producing multilayer ceramic capacitors in the form factor of these substrates. The calculations of capacitance for these capacitors are shown in Fig. 6, and the processes being considered in 1959 are listed in Fig. 7. Doctor blading was selected because it had the potential for making the thinnest layers. The binder chosen was a polyvinyl chloride acetate and a plasticizer, which were dissolved in a methyl ethyl ketone solvent plus a wetting agent. Screening of the electrodes was accomplished with commercial palladium pastes, which were available at that time. The problem of lamination was difficult to solve, but eventually a solution was found by Gyurk (1965) with the use of a heated press. Individual capacitors

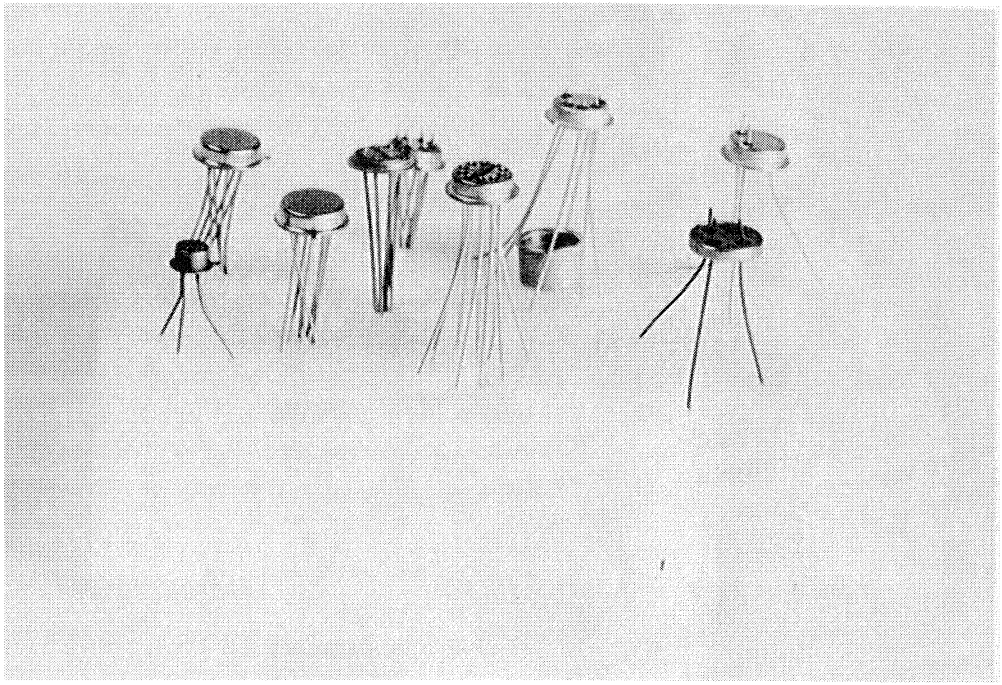


FIGURE 3 Glass-to-metal sealed headers, showing the various sizes and number of leads per header and caps.

were then cut from the laminates and sintered in air at temperatures between 1200 and 1400°C. This process spawned the current laminated ceramic capacitor industry.

In 1960, engineers from the RCA plant in Camden, New Jersey, asked their coworkers in the Micromodule Laboratory in Somerville, New Jersey, to develop a package for quartz crystal oscillators, which were to be used in military helmet radios. This was the first laminated ceramic package to be built with an alumina ceramic and molybdenum-manganese metallization. The alumina slurry was prepared with a polyvinyl butyral binder, plasticizer, and solvents, which were used to cast the green sheets. The Mo-Mn paste, when sintered, adhered well to the ceramic, which provided excellent hermeticity. The quartz crystal was mounted on the two tabs shown in Fig. 8, and the entire package withstood vibration, thermal, and humidity tests, which is described by Schwartz (1961). Because of the breakthrough with the quartz crystal oscillator, other packages were built for transistor

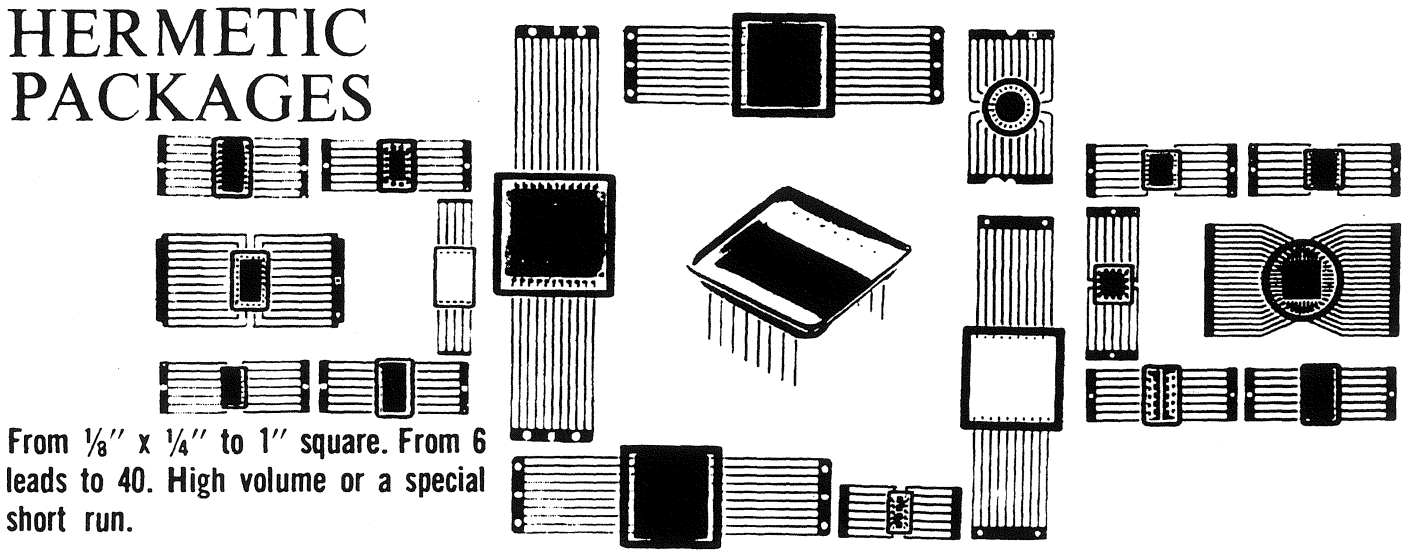


FIGURE 4 Hermetic flat packs, showing the various sizes up to one inch square.

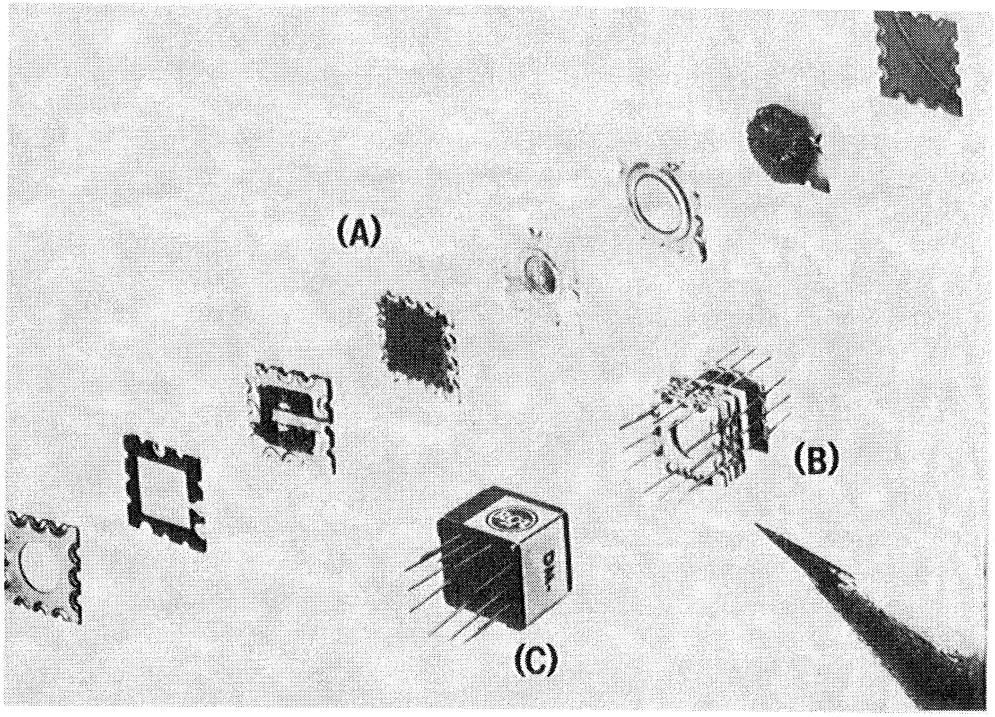


FIGURE 5 (A) Micromodule wafers. From left to right: end wafer, capacitor, electrolytic capacitor, resistor, diode, transistor, inductor end wafer; (B) assembled module with riser wires; (C) encapsulated module. (Each wafer is 0.3 by 0.3 in. square.)

circuits, as shown in Fig. 9. Alumina ceramics and Mo-Mn metallurgy were also used to make these new packages.

The next invention occurred in the same RCA laboratory, in late 1960, when the concept of a "via" was created by Stetson (1965). A *via* is a hole punched in the ceramic green sheet and then filled with a metal paste. These vias were used to interconnect several layers of conductors, as shown in Fig. 10. Thin metal films were deposited and then etched on the surface of this module to make the many interconnections. These etched films were then connected to the vias for making the electrical connections from layer to layer within this module. The concept established the means for making many interconnections in a ceramic substrate and has subsequently been used in later modules.

1958

Micro-Module Program Needed, in a 0.3 In. by 0.3 In. Ceramic Wafer Form, the Following:

1. **Precision Capacitors with up to 3000 pf and 50 Vdc Ratings**
2. **General Purpose Capacitors with up to 300,000 pf and 50 Vdc Ratings**

$$C = \frac{.224\ KAn}{T}$$

C = Capacitance (pf)
K = Dielectric Constant
A = Electrode Area (Sq. In.)
N = Number of Layers
T = Layer Thickness (In.)

For (1) $K \simeq 30$
$A \simeq .04$
$T \simeq .001$
$N \simeq 11$

For (2) $K \simeq 3000$
$A \simeq .04$
$T \simeq .001$
$N \simeq 11$

FIGURE 6 Capacitance calculations made in 1958.

1959

Process	Estimated Minimum Thickness (10^{-3} In.)	Concerns
• Pressing	5	Too Thick
• Extruding	3	Control
• Extruding (Plus Microtome)	1	Lamination
• Spraying	3	Shorts
• Doctor Blading	Unknown	Lamination
• Screening	1/2	Shorts
• Electrophoresis	1/10	Shorts
• Electroplating With Anodization	10^{-3}	Voltage Rating
• Sputtering or Evaporating	10^{-3}	Voltage Rating

Decision: Doctor Blading
Problems: 1. How to Cast Thin Sheets
2. How to Metallize
3. How to Laminate
4. How to Interconnect Layers

FIGURE 7 The methods which were considered in 1959. Doctor blading was selected as the most promising process.

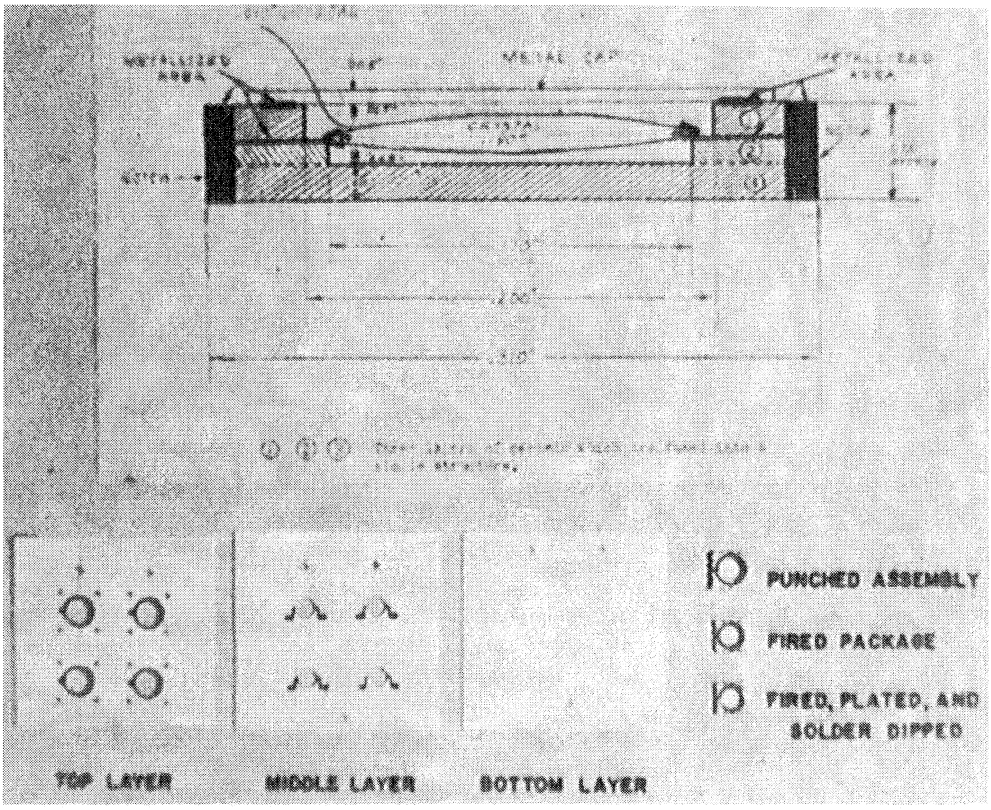


FIGURE 8 Quartz crystal oscillator package, which was a three layer structure. The electrode configurations were screened onto the green sheets, then the package was laminated and sintered. After sintering the parts were plated and solder dipped. The quartz crystal was mounted on the two tabs shown in the cavity and the package sealed.

The next application was a high-speed computer, which the military called Project Lightning. It employed small diode and transistor packages, which were made with green sheets of alumina and Mo-Mn. The Mo-Mn green sheets were laminated to the outer surfaces of the alumina sheets. Then, washerlike structures were punched from the original laminates and sintered to provide hermetic seals when brazed to the electrodes of these packages. A schematic drawing of a small transistor package is shown in Fig. 11.

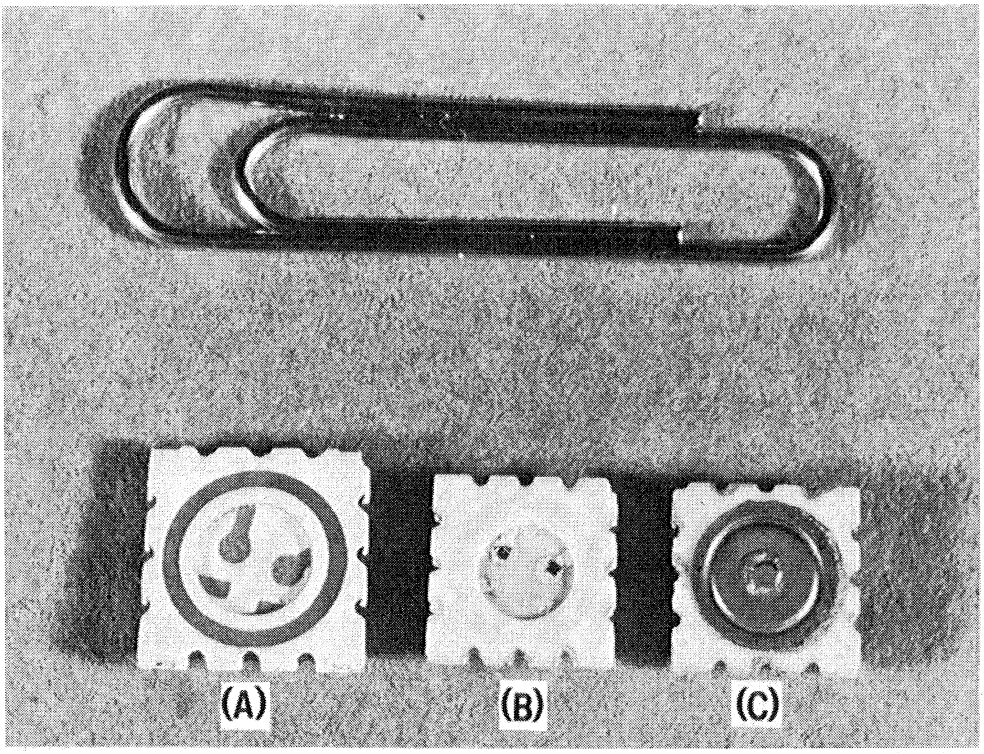


FIGURE 9 Transistor package: (A) Laminated structure, (B) sintered substrate and (C) sealed package.

As a result of the Micromodule Project and Project Lightning, new technologies were established to provide the basis for the next generation of computer packaging. These processes set the stage for the evolution of modern electronic packages for the computer industry.

1.3 IBM SYSTEM TECHNOLOGIES

During the period 1961-1965, IBM developed its System 360 computers, which used the solid logic technology (SLT) module. This module utilized a 0.455 by 0.455 in. 96% alumina ceramic substrate that contained up to 16 holes into which copper pins were swaged. Thick films of noble metal conductors and resistors were screen printed in various patterns to provide the mounting pads for the transistors and diodes,

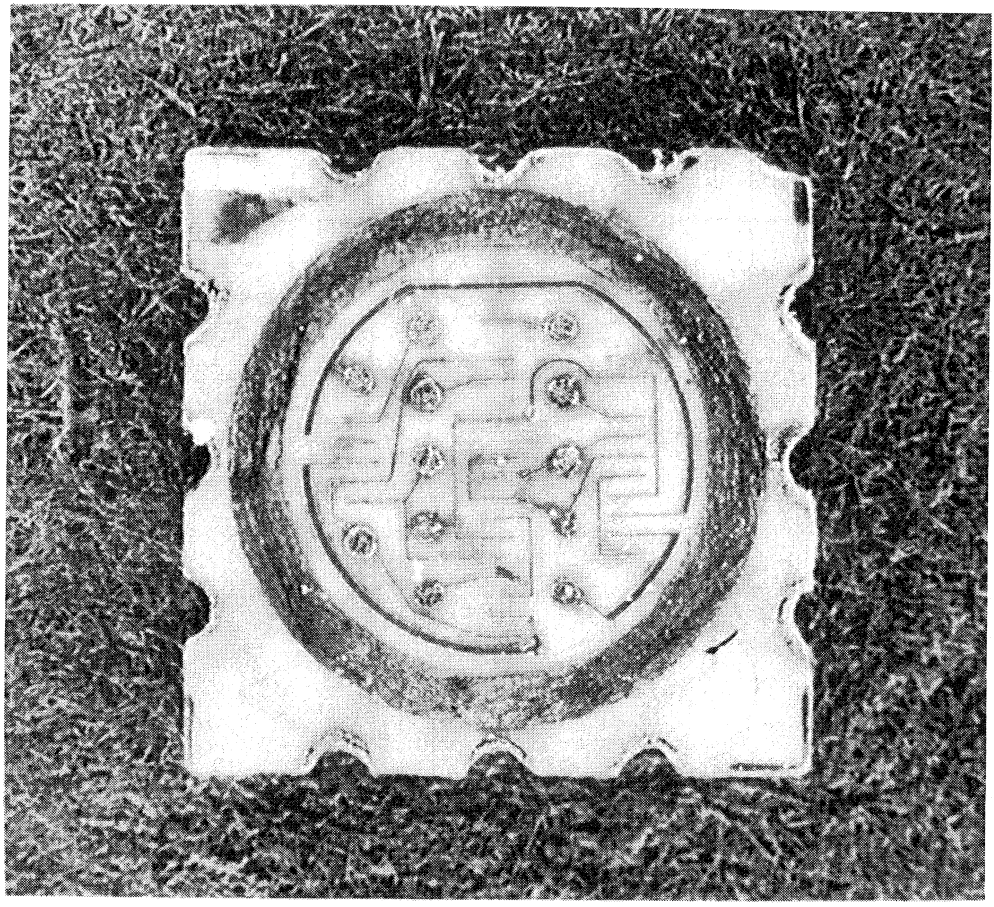


FIGURE 10 Micromodule substrate, which interconnected several unipolar transistors with etched thin films to the vias in the ceramic substrate. The substrate is 0.3 in. square, and shows how the connections are made with thin metal films.

as shown in Fig. 12. Glass dams were provided so that the solder on the copper balls could not flow up the conductor patterns. Figure 13 shows a transistor chip with a glass coating, so that this module did not have to be hermetically sealed. For a full description of the SLT module, see Davis (1964).

The next development, introduced in 1970, was called the monolithic systems technology (MST), as shown in Fig. 14. This module mounted

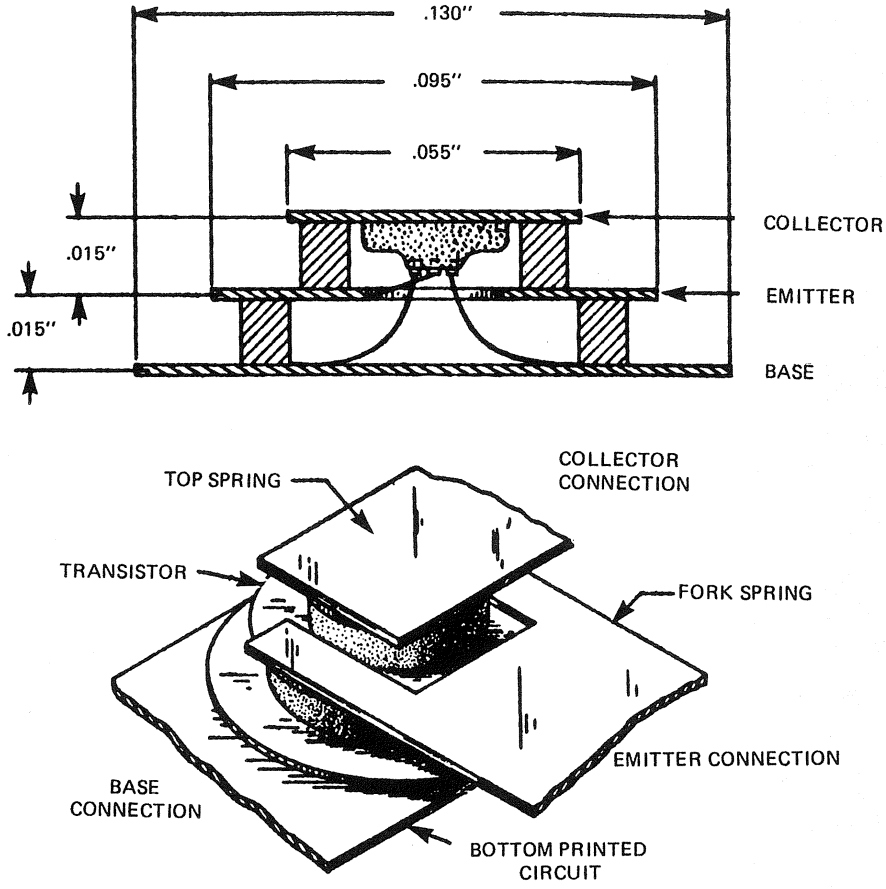


FIGURE 11 Project lightning transistor package, showing the very small size.

integrated circuit chips, and the method of joining was changed from solder-coated copper balls to 95:5 Pb-Sn solder pads, which had diameters of the order of 5 mils. In Fig. 15A, a typical solder connection is shown for this chip. Glass dams were again used to prevent the flow of solder onto the conductors, as described by Miller (1969).

A larger substrate was used in 1975 for the metallized ceramic (MC) module. In this technology, thin films of chromium and copper were evaporated onto the surface of the substrate to form fine line patterns. The sequence of depositions was Cr-Cu-Cr, where the top Cr layer was etched back to prevent the solder from flowing onto the lines.

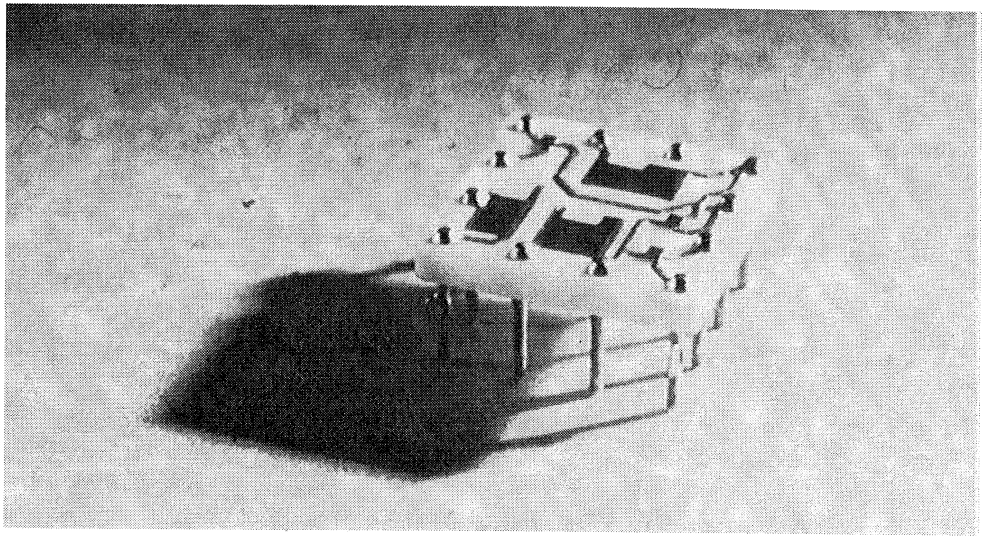


FIGURE 12 SLT module, with transistors and resistors on the surface.

The larger substrate also permitted the use of more pins. This module is still in use for IBM computers (Fig. 16) and is reported by Bendz (1982).

In 1979, the multichip module (MCM) was introduced by IBM, using the multilayer ceramic technology. This module held up to 9 chips, had up to 23 layers, and was hermetically sealed. It was air cooled (Fig. 17), and is described by Blodgett (1980).

The evolution of density and performance in IBM module technologies is depicted in Fig. 18. Circuit delay times decreased over one order of magnitude, and circuit densities at the module level increased over four orders of magnitude. Also note that improvements occur in much shorter intervals of time. See Table 1 for additional details of these systems.

The reliability of these packages had to improve with each advance in technology. The original data were reported by Schwartz (1969), and additional information was obtained from Shapiro (1986), which is presented in Table 2. To date, the MLC technology has not had a single field failure, which is an outstanding achievement.

TABLE 1 Ceramic Modules in IBM Systems

	SLT	MST	MC	MCM	TCM	MCM	TCM
Year started	1965	1970	1975	1979	1980	1983	1985
Ceramic	96% alumina			92% alumina			
Metal	Au-Pd and Ag-Pd pastes		Thin films Cr-Cu-Cr	Mo paste and Ni-Au plating			
Sizes (mm)	11.6 × 11.6		28 × 28 36 × 36	35 × 35 50 × 50	90 × 90	64 × 64	107 × 118
Layers	1, 2	1, 2	1	23	33	32	36
Chips	7	4	4	9	133	36	100
I/O	16	16	120-170	361	1800	882	1800

TABLE 2 Reliability Trends

Technology	Year introduced	Failure rates (per 10^3 hr)
Discrete devices	1950	10^{-1}
Micromodules	1958	10^{-2}
Thick films	1948	10^{-3}
Diodes, transistors	1960	10^{-4}
Integrated circuits	1970	10^{-5}
LSI	1975	10^{-6}
VLSI	1980	10^{-7}

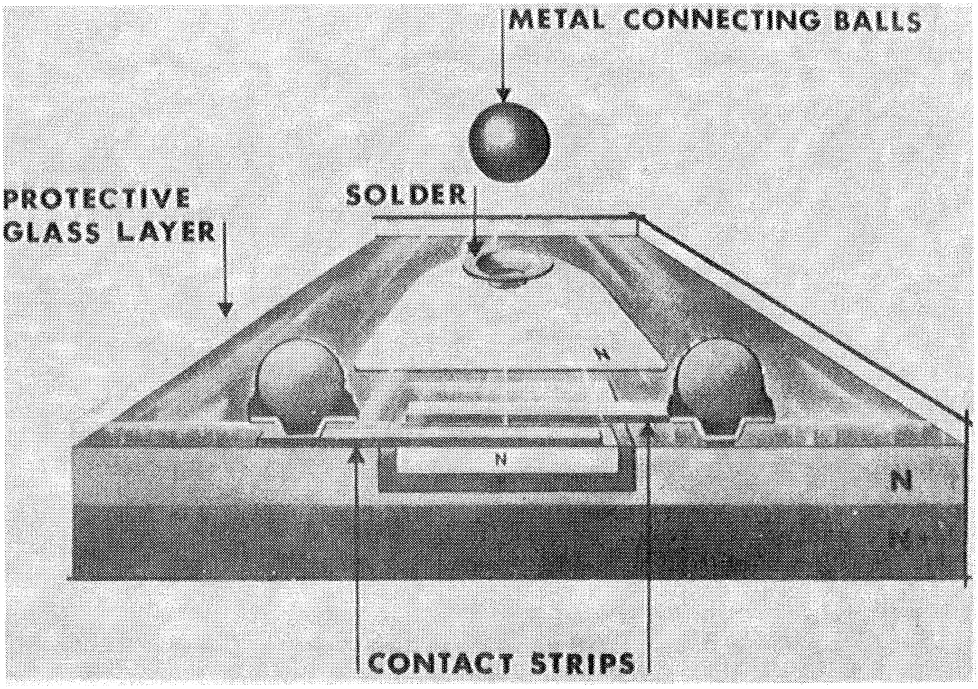


FIGURE 13 SLT transistor with protective glass layer and solder-coated copper balls on its surface.

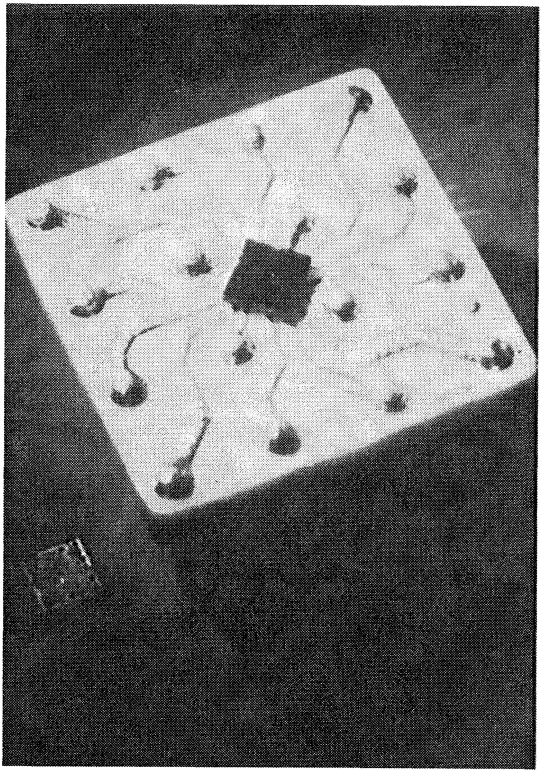


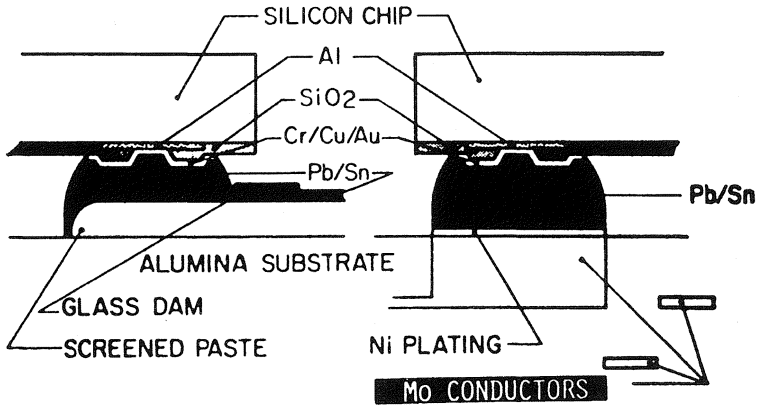
FIGURE 14 MST module, with an integrated circuit chip mounted on its surface.

1.4 MULTILAYER CERAMIC TECHNOLOGY

The thermal conduction module, hereafter referred to as TCM, currently being used in IBM high end computers, is one of the most advanced ceramic modules. The TCM provides the high-density wiring needed in large-scale computers. A knowledge of its characteristics, specifications, and manufacturing processes will acquaint the reader with some of the basic principles involved in the MLC technology. The steps in the total process are listed in Fig. 19 and are described by Blodgett and Barbour (1982) and Burger and Weigel (1983).

The alumina and glass powders are mixed with a polyvinyl butyral binder, plus a plasticizer and two solvents, in a ballmill, where the ceramic powders are dispersed and the glass powders are ground down to a finer particle size. The slurry is then transferred to a

C-4 JOINING MICROSOCKET JOINING



(A) (B)

FIGURE 15 (A) C-4 joining (controlled-collapse-ship-connection), using 95-5% lead-tin solder pads for the interconnections. (B) Microsocket joining, which uses the same lead-tin solder, but with the MLC structure.

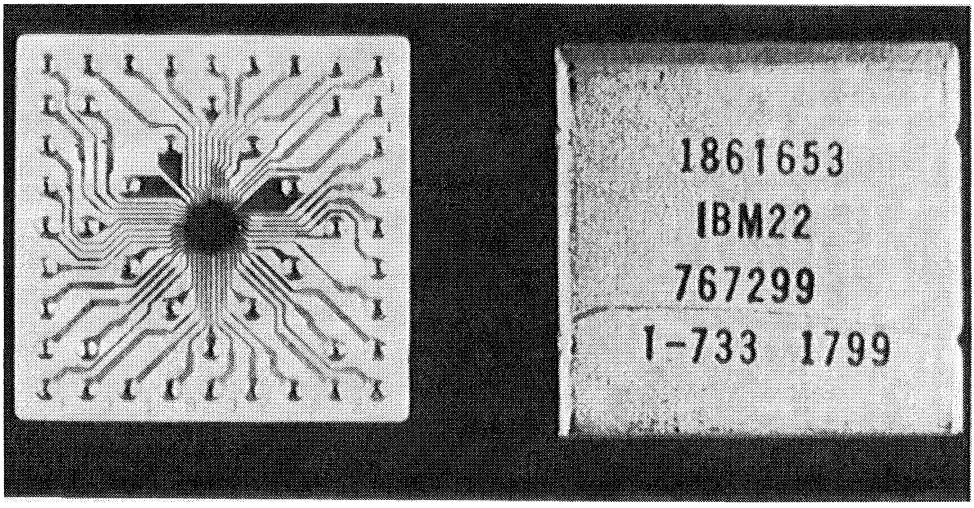


FIGURE 16 MC module, with an enlarged substrate in order to accommodate up to four integrated circuit chips.

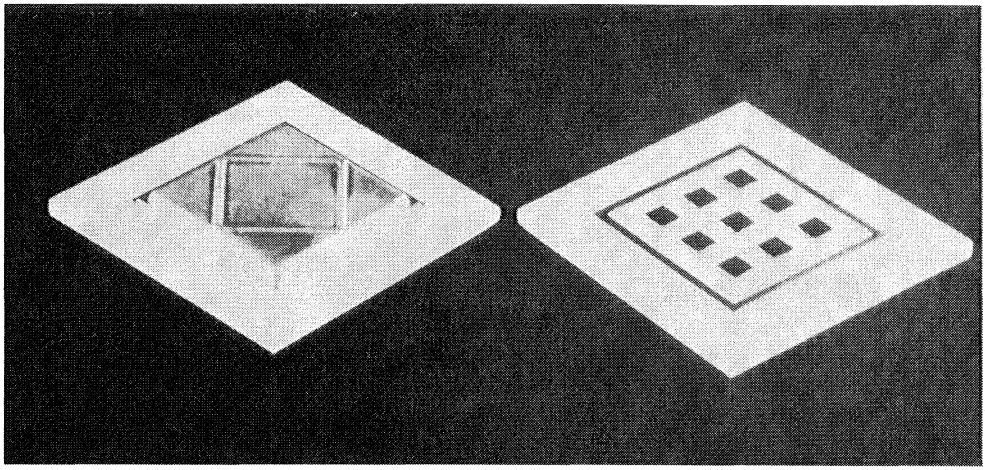


FIGURE 17 MCM substrates: (Left) hermetically sealed with a cover; (Right) substrate with up to nine chips on its surface.

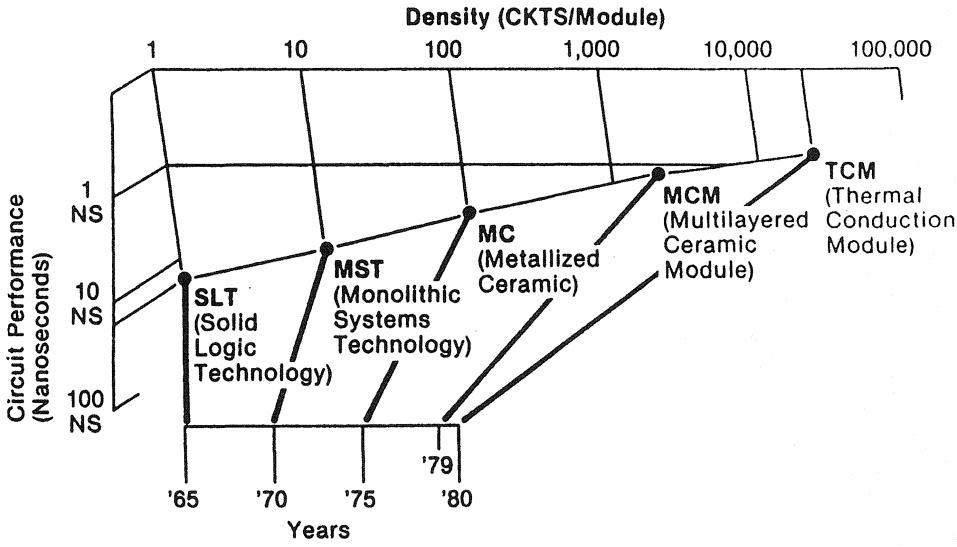


FIGURE 18 Evolution of circuit performance and density in IBM module technologies.

PROCESS

1. Ball Mill Slip (Aluminas)
2. Doctor Blade Tape on Mylar
3. Dry, Strip and Reel
4. Blank
5. Punch Holes (Location, Vias, Etc.)
6. Screen Mo (or W) Pastes and Dry
7. Stack and Laminate
8. Size (Cut)
9. Sinter
10. Plate
11. Braze (Pins, Flange)
12. Mount Chips
13. Seal

(Testing Steps Omitted)

FIGURE 19 MLC process, listing the thirteen steps involved in making a substrate.

tank in the cart, where it is agitated and filtered. See Fig. 20 for a schematic of this system.

This slurry is then poured into the reservoir, which is used to maintain a constant fill level. The casting has to be done under carefully controlled conditions so that the green sheets will not distort or crack. A schematic of the reservoir and doctor blade is shown in Fig. 21.

Figure 22 shows a picture of the doctor blading system in which the green tapes are dried in the drying chamber and then stripped from the plastic and reeled onto several spools, each 200 mm wide. The actual shrinkage of the material is determined by punching out squares of the green sheets, laminating them, and then sintering these laminates.

These green sheets are then passed through a blanking tool, which inspects the ceramic tapes with a laser system. Any defects are advanced out of the range of the punch, and then 185 mm^2 blanks are punched from the tape, as shown in Fig. 23.

In the next step, location holes and vias are punched with an automatic tool, which has a hundred or more individual punches in its head, which are computer controlled for specific patterns. After the via holes are punched, they are inspected with photodiodes (Fig. 24).

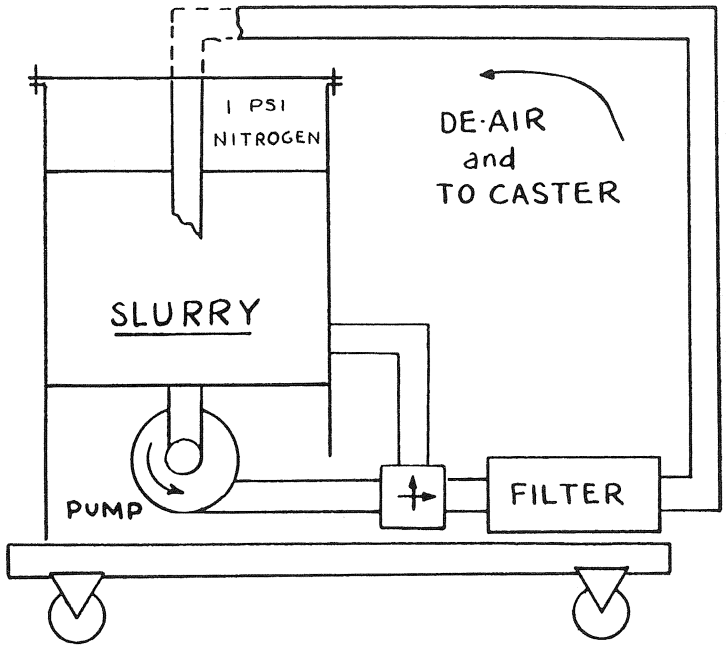


FIGURE 20 Slurry cart and storage, where the slip is being pumped, filtered and de-aired.

The next step is to screen the Mo pastes through a Mo mask with the use of a pressure nozzle screening tool. Each layer has a different pattern, and after screening the pastes onto the green alumina sheets they are dried in an oven and repaired, if necessary. These sheets are then passed through an inspection station run by robots. This equipment can distinguish between the black and white colors of the metallurgy and alumina. The various patterns used in the TCM substrates are shown in Fig. 25. If the metallurgy is not balanced from top to bottom, the substrates can camber, distort, or crack.

The stacking process uses a computer selection method to place all the sheets in the correct sequence. The next step is to transfer this stack to the lamination press, where the press cuts the green sheets and then applies heat and pressure to complete the lamination process (see Fig. 26).

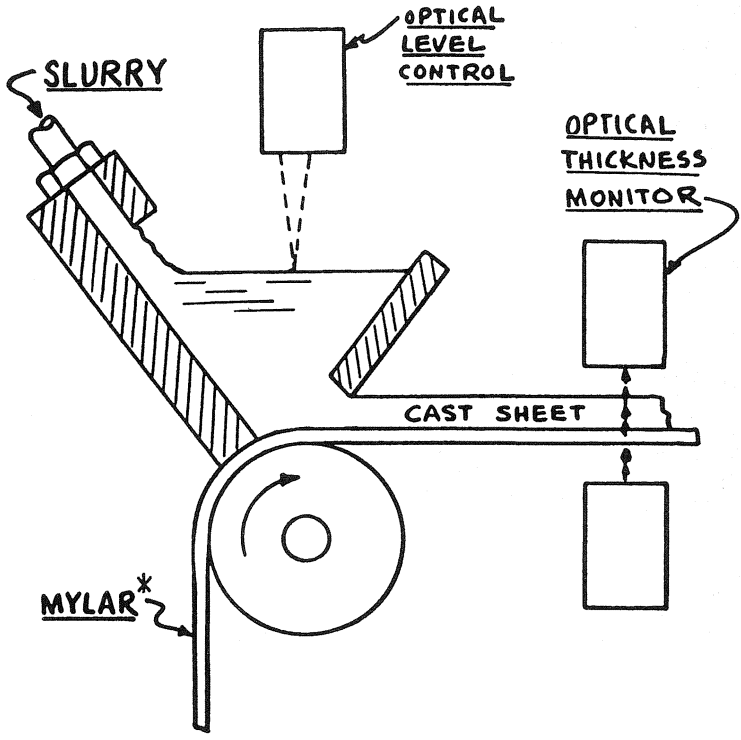


FIGURE 21 Casting, showing the doctor blade, slurry feed, level control, thickness monitor and cast sheet.
*Mylar, Dupont registered trade name.

In all prior steps the substrates are held in position with their location holes. For the sizing operation, the substrates are held in place with a vacuum chuck and then cut with a silicon carbide saw.

The substrate is now ready for sintering in either a batch or continuous wet hydrogen atmosphere furnace, where the thermal cycle has to be very accurately controlled with regard to temperature and atmosphere. The atmospheres have to take into account the oxidizing conditions for binder burnout and bring the substrate to its complete density. Figure 27 shows the mechanisms that have to be considered for binder burnout. These substrates are sintered at temperatures in the range of 1525-1575°C in a wet hydrogen atmosphere, as described by Chance (1970).

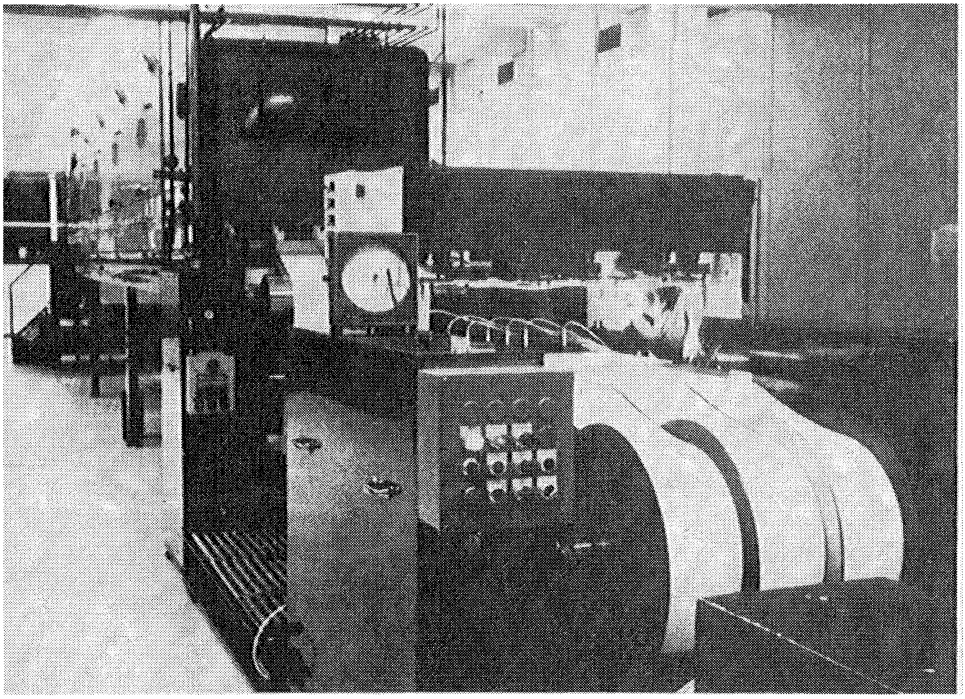


FIGURE 22 Modern doctor blading system, showing the drying chamber and three green sheets being reeled on three drums.

After sintering, these parts are plated in a continuously automatic plating system. First, a low-stress nickel film is electrolessly plated on the patterns printed on the surface of the substrate. Then a thin gold coating is applied, followed by a heavy gold layer on the engineering pads, as shown in Figs. 28, 29, and 30. An engineering change pad is used to alter the wiring within a substrate, as shown in Fig. 30. The connector line between the via and pad is cut with a laser, and the heavy gold is then needed to achieve wire bonding to these pads. A cross section of a TCM module is shown in Fig. 31.

In the next operation, the pins and flange are brazed to the substrate, which is done with a gold-tin alloy in a hydrogen atmosphere furnace at a temperature of about 400°C.

IBM uses these processes, and other companies also use this technology, but with other materials.

At Kyocera, a 96:4 alumina-glass ceramic with a tungsten metallurgy is used, and it is sintered in wet hydrogen in the range of

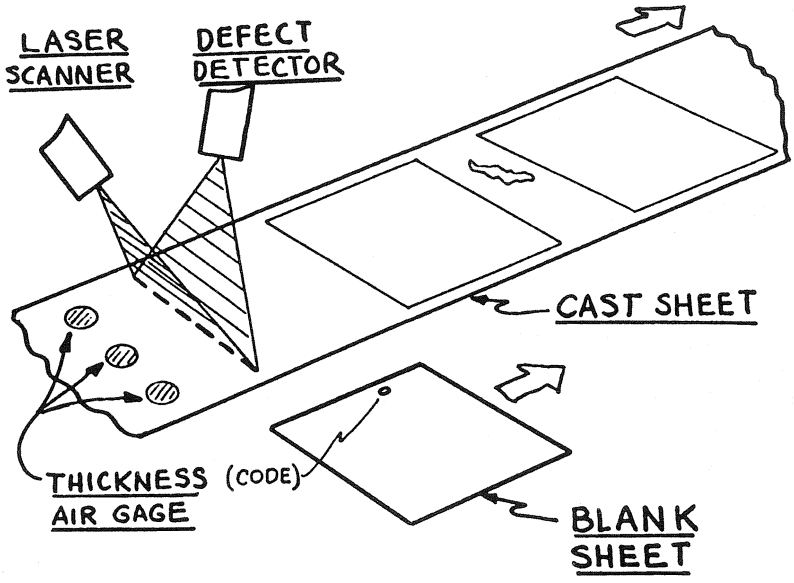


FIGURE 23 Blanking process, where the green sheets are measured for thickness and then scanned for defects, and blanks are punched and coded.

1500-1600°C. At NEC, a 55% alumina-45% glass ceramic with gold electrodes is produced, which is sintered in air below 1000°C (Shimada, et al., 1983).

1.5 CHIP JOINING METHODS

The controlled-collapse-chip-connection (C-4) permits many solder joints to be made in a single thermal process. These connections have been very reliable in regard to the size of the chips at each step in the series of IBM module development. The actual process begins with a tool that positions these devices, using a flux to hold them in place, on the substrate. The pads on the chips are coated with a 95:5 Pb-Sn solder, then passed through the furnace in a forming gas atmosphere and aligned owing to the surface tension of the solder. The cycle time through this furnace, which is held at 340°C, is about 30 min. A bonded chip is shown in Fig. 15B.

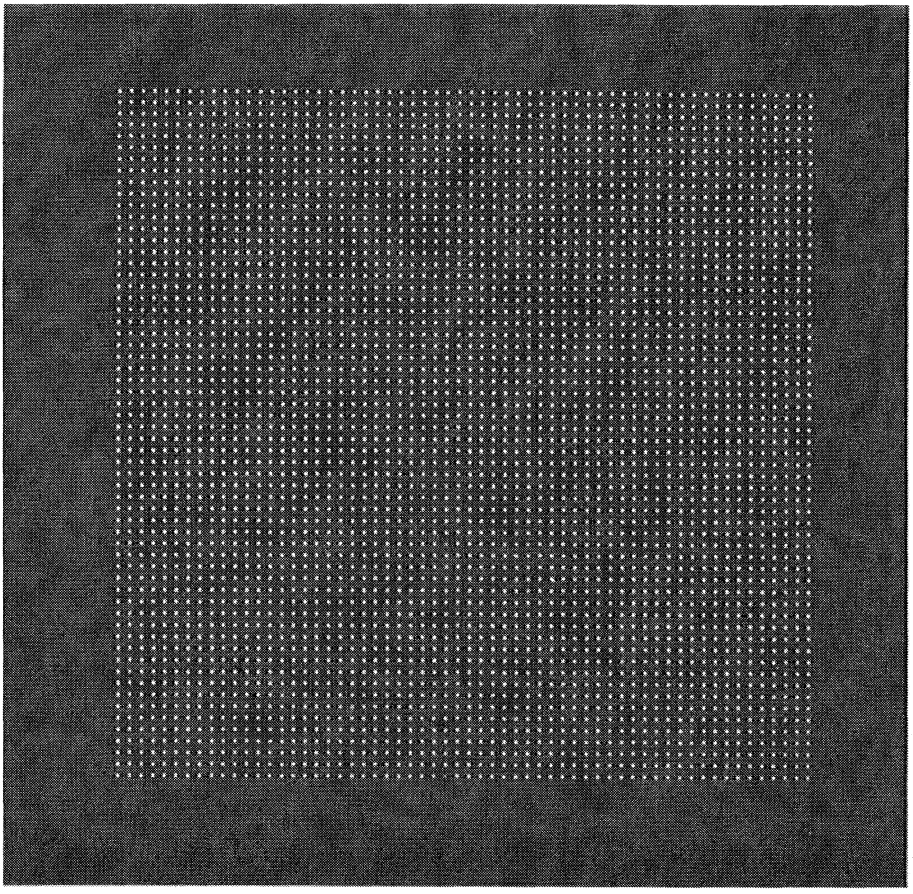


FIGURE 24 Green sheet, with location holes, 3600 vias and 0.007 in. thick.

Another chip-joining method is wire bonding. Each chip is back-bonded to the substrate with either a silver-loaded epoxy or a gold-silicon eutectic alloy. The connections from the chip to the substrate are made with 1-3 mil diameter aluminum or gold wires.

Tape automated bonding (TAB) is another process used at this time. A TAB is a copper foil that has been etched to fabricate many connectors, which may be gold plated. These chips are usually encapsulated with one of a variety of resins.

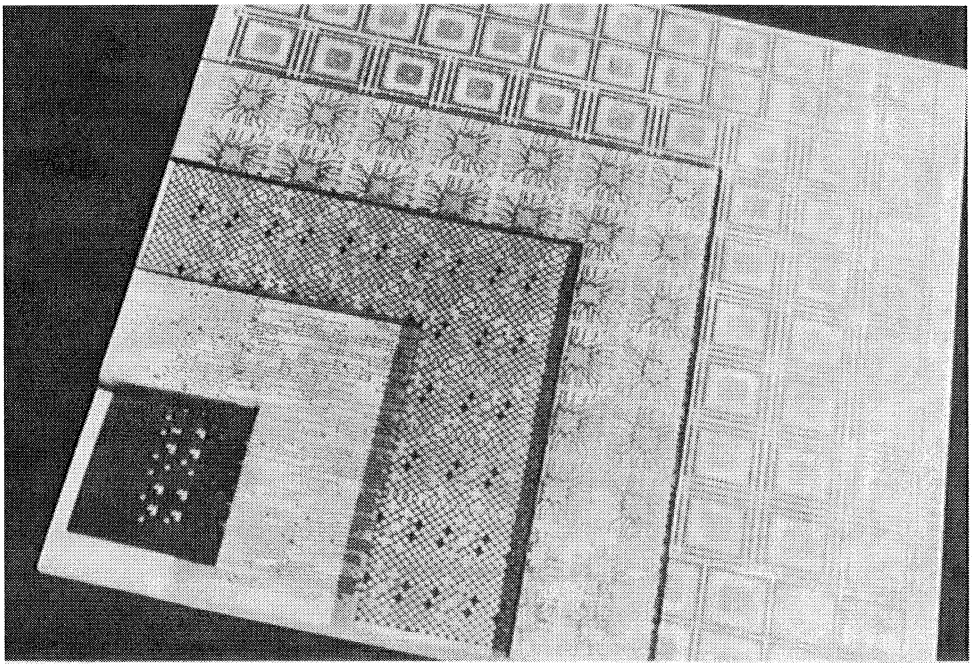


FIGURE 25 Patterns used in TCM: top layer: C-4 connections and engineering change pads; fan-out layer; reference patterns; circuit lines; power planes; pin pads (not shown).

Some of the chips now in use in IBM MLC modules are shown in Fig. 32. The device in Fig. 32A is a 9 Kbit array chip; in Fig. 32B, a 1100 circuit multiplier chip; in Fig. 32C, a 704 circuit logic chip. The captions describe their respective functions. Figure 33 shows a 36 chip MCM with its heat sink exposed. Figure 34 shows this module being inserted into a printed circuit board. The specifications for this module are also given in Table 1.

Chip replacements can be made by mechanically removing selected units and then putting them through a normal reflow cycle. They can also be replaced individually, with the use of a special heating tool.

The stress constraint is concerned with the size limit of silicon chips, which determines the fatigue failure of the solder pads. Each time the computer is turned on and off, the modules are heated and cooled. The resulting plastic strain E_p in the solder pads equals

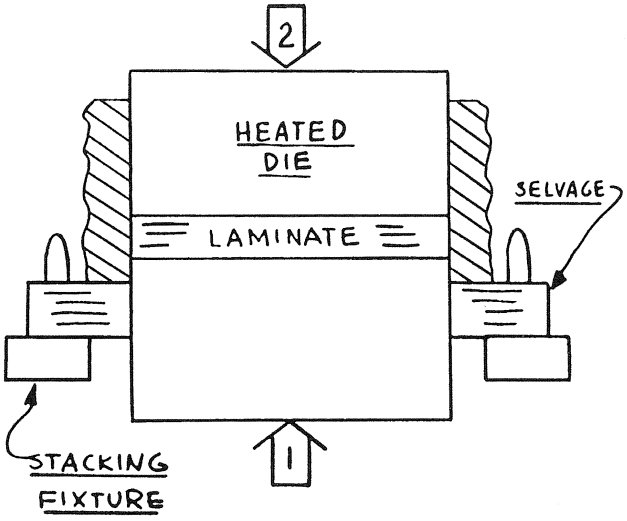
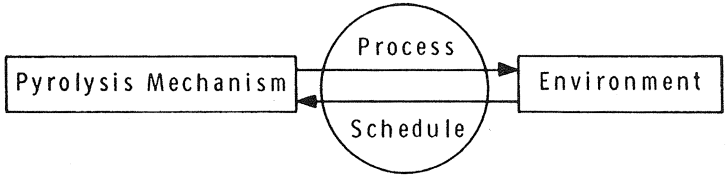


FIGURE 26 Lamination die, which cuts and laminates the green sheets.



Pyrolysis Mechanism	Environment
Sublimation	Oxidation - Reduction
Fractionation	Temperature - Time
Oxidation	Pressure

FIGURE 27 MLC binder pyrolysis studies.

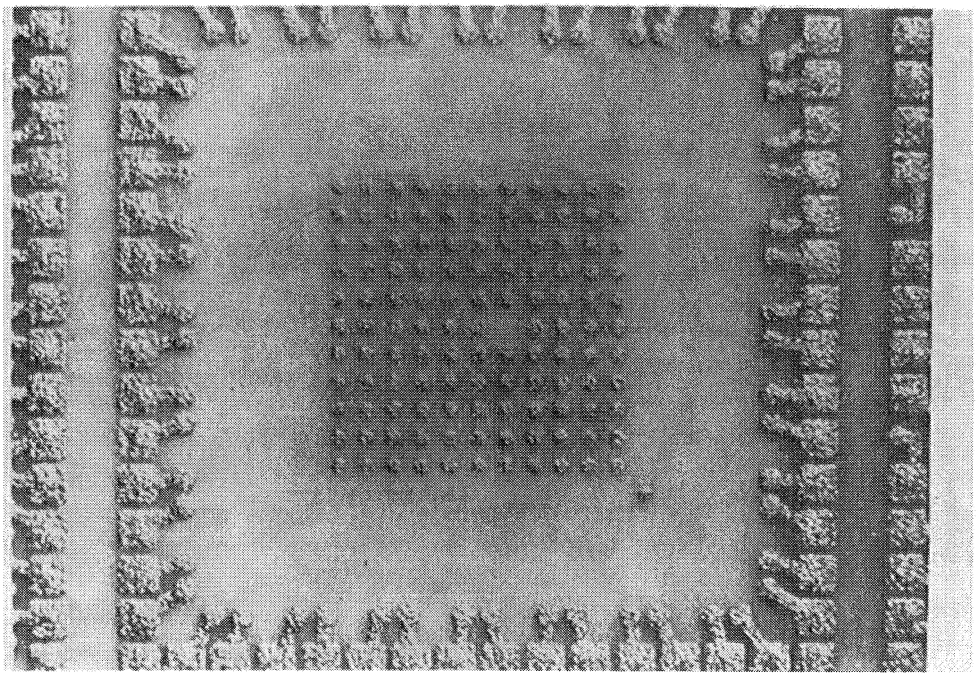


FIGURE 28 Microsockets and engineering change pads.

$$E_p = \Delta TCE \cdot \Delta T \cdot \frac{D_{np}}{H} \text{ cm/cm} \quad (1)$$

where ΔTCE is the difference between the thermal expansion of the silicon and the ceramic materials, ΔT is the change in temperature in degrees Celsius, D_{np} is the distance in centimeters from the neutral point on the chip, and H is the height in centimeters of the solder pad, as reported by Goldmann (1969).

Manson (1966) related the number of cycles to failure N_f according to the following equation:

$$N_f = \frac{C}{E_p^2} \quad (2)$$

where C is a constant determined for each system. As LSI chips become larger it will be necessary to find new ceramic materials with more closely matched thermal expansions to that of the silicon.

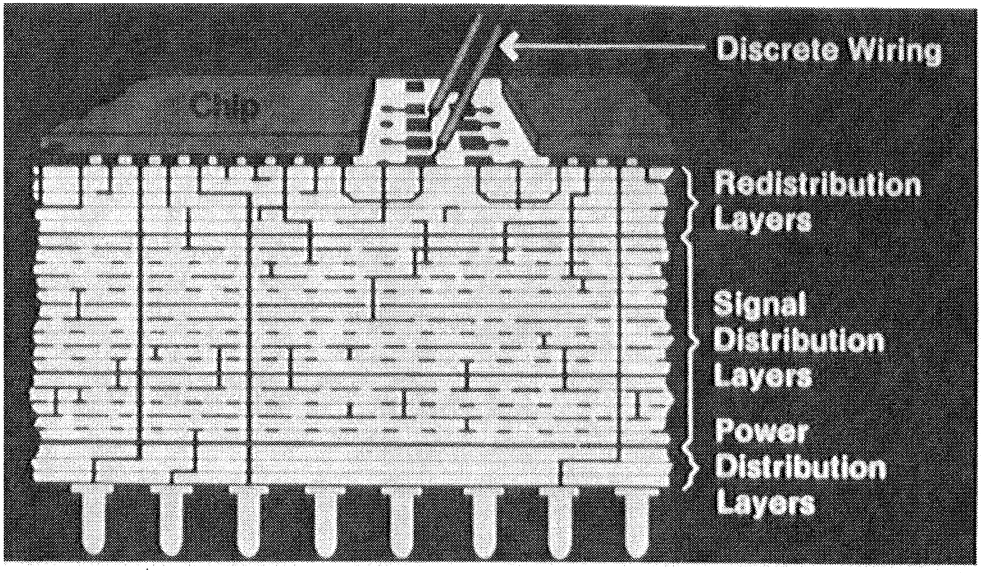


FIGURE 29 Schematic for showing how the engineering changes are made.

1.6 MODULE FUNCTIONS

A TCM module requires special electrical and physical characteristics to accomplish its mission. These functions include electrical transmission lines, power distribution, hermetic seals, cooling, pin attachments, and engineering change capability.

1.6.1 Transmission Speeds

The primary concern in a TCM module is to increase the speed of the signals through the substrate, which is controlled by the distance a pulse must travel and the dielectric constant of the media through which it passes. These parameters have been described by Chance and Wilcox (1971). Distance is the most important parameter because it has a linear relationship to the time delay. The AC considerations are given by the following equation:

$$T_d = \frac{L\sqrt{K}}{C} \text{ nsec/in.} \qquad (3)$$

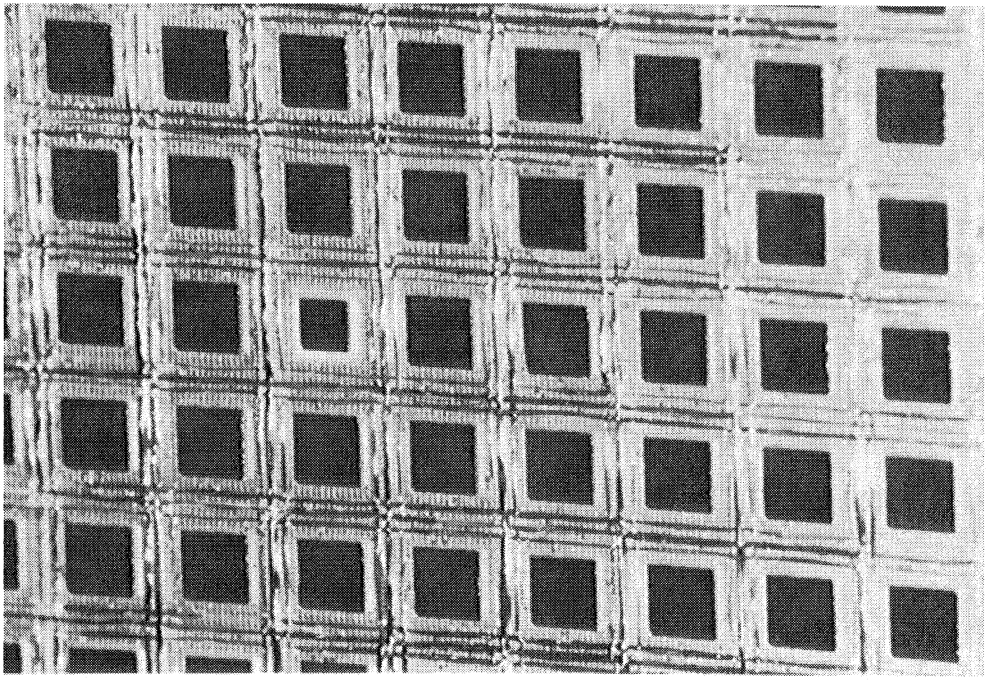


FIGURE 30 Engineering change wires and chips.

where T_d is the time delay in nanoseconds, L is the distance a signal must travel in inches, K is the relative dielectric constant of the ceramic, and C is the speed of light in inches per second. Examples of time delays due to the relative dielectric constants of various ceramics are listed in Table 3. Referring to Fig. 35, the distances signals must travel can be controlled by varying the grids from the silicon chips to the MLC substrate to the multilayer printed circuit board. An entire level of packaging, the card, was eliminated through the use of the MLC substrate, as reported by Balderes and White (1985).

The characteristic impedance for conductors with elliptical cross sections must meet the design criteria for MLC lines within the ceramic and can vary between 35 and 100 Ω for transistor circuits, as reported by Sands and Wilcox (1969). The characteristic impedance for a transmission line is given by the following equation:

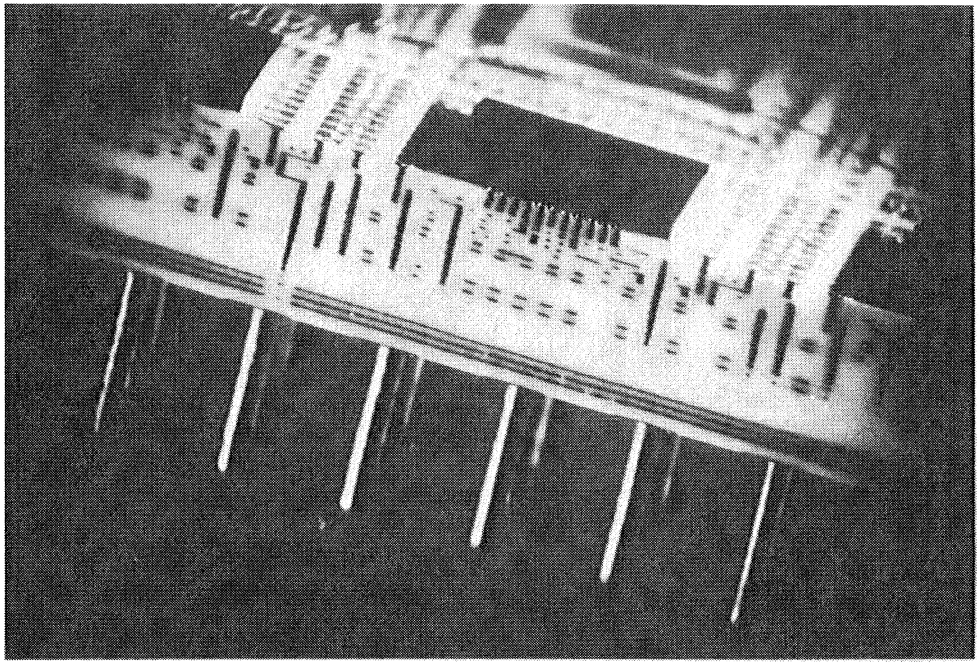


FIGURE 31 Cross-section of TCM, showing wiring patterns and chips.

$$Z_0 = \frac{\sqrt{L}}{C}\ \Omega \tag{4}$$

where L is the inductance and C is the capacitance of the line. As the relative dielectric constant of the ceramic is reduced, thinner layers have to be used for the same impedance.

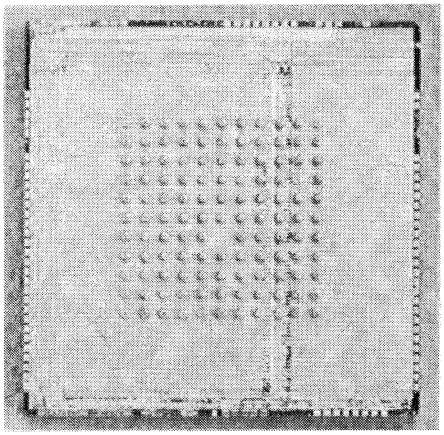
The coupling coefficient (CC) between lines is given by the following equation:

$$CC = \frac{1}{1 + C_1/C_2} \tag{5}$$

where C_1 is the line capacitance to ground and C_2 is the line-to-line capacitance. Cross-talk can occur if these lines come too close to each other because the capacitance (CC) increases due to an increase in C_2.

TABLE 3 Ceramic Materials

Ceramics	Dielectric constant	Thermal conductivity (W/M °C)	Thermal expansion ($\times 10^{-6}$ °C^{-1})	Strength (MPa)	Delay time (10^{-9} sec/in.)
Current					
96% Alumina, 4% glass	10.2	20.9	7.1	276	0.27
92% Alumina, 8% glass	9.5	16.7	6.9	315	0.26
55% Alumina, 45% glass	7.5	4.2	4.2	296	0.24
Future					
AlN	8.8	260	4.4	276	0.23
Si_3N_4	6.0	33.5	3.0	586	0.21
SiC	40	340	3.1	400	—
Mullite ($3Al_2O_3 \cdot 2SiO_2$)	6.2	10	4.5	165	0.21
Cordierite ($2MgO \cdot 2Al_2O_3 \cdot 5SiO_2$)	6.0	10	1.6	103	0.21



(A) Memory

FIGURE 32 Silicon chips used in IBM systems, for (A) memory, (B) multiplier, and (C) logic.

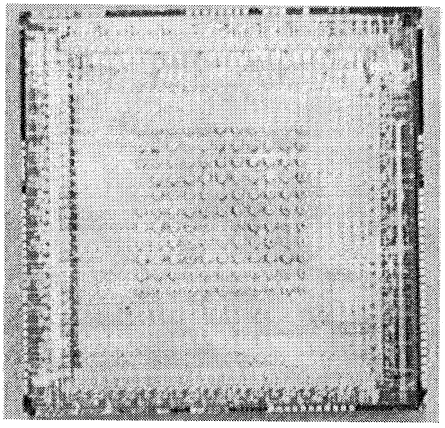
The relative dielectric constant of the ceramic is an important parameter in this equation. It can be lowered by decreasing its electronic, dipole, and ionic polarizabilities, atomic numbers, bond strength, and density. Glasses, therefore, would tend to have lower dielectric constants than crystalline structures. Any technique that would increase the specific volume of the material could be beneficial. The constraint, however, would be lower strength.

1.6.2 Power Distribution

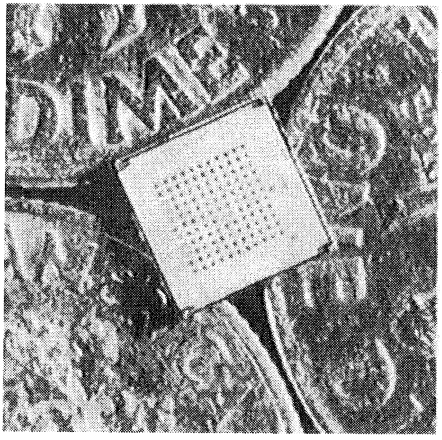
The conductivity of the metal electrodes is a predominating parameter for power distribution. As the dimensions of the modules become smaller, the conductivity of the metallurgy has to increase. The resistance of a conductor R is given by the following equation:

$$R = \frac{\rho L}{A}\ \Omega \qquad (6)$$

where ρ is the resistivity in ohm-centimeters, L is the length in centimeters, and A is the cross-sectional area in square centimeters of



(B) Multiplier



(C) Logic

the line. A higher line resistance produces voltage drops and localized heating, which can affect device switching behavior.

Alternatives to higher conductivity metals are decoupling capacitors that can be used on the surface of the substrate. Also, direct bussing lines can be considered when the modules become too small for direct access by the wiring.

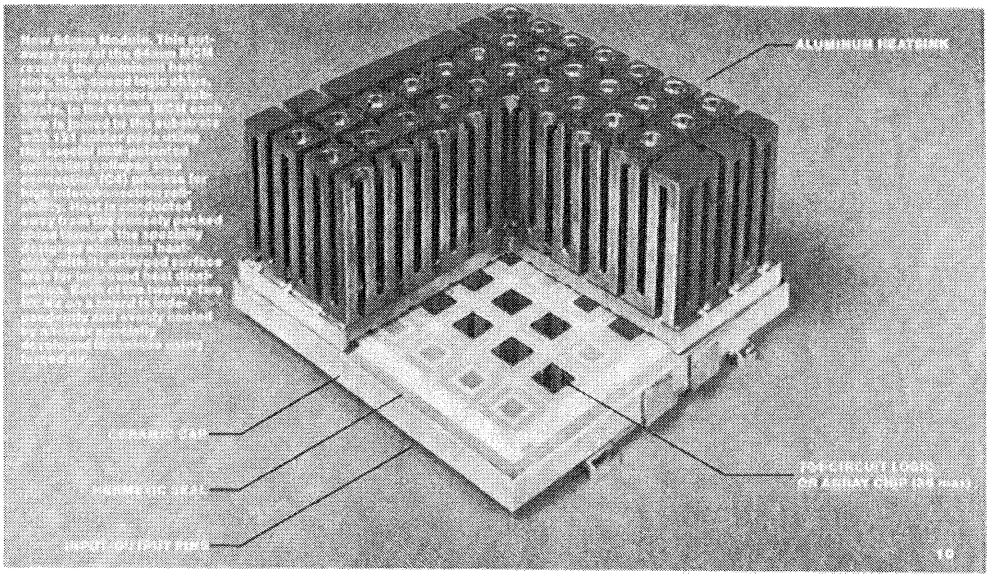


FIGURE 33 New MCM 36 chip, 64 mm square module with heat sink attached.

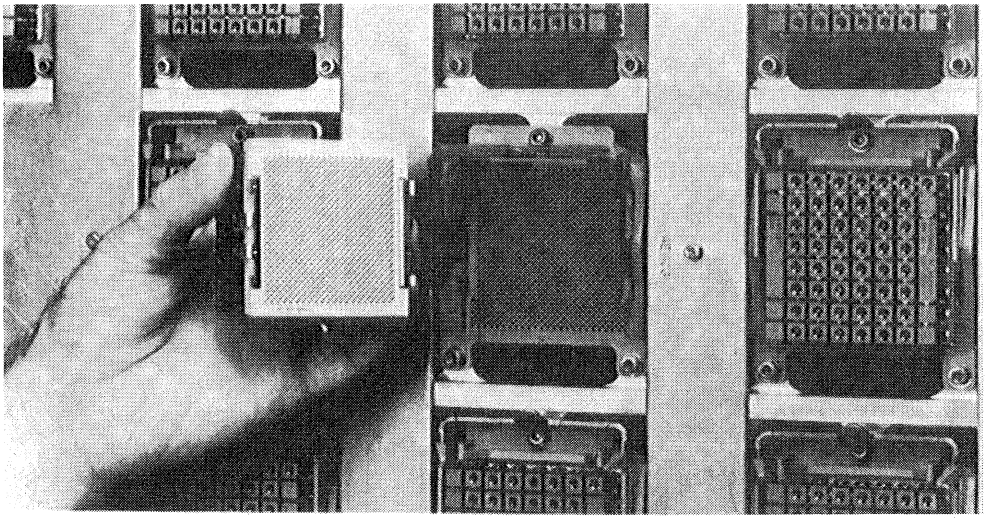


FIGURE 34 New MCM 36 chip module being inserted into a printed circuit board.

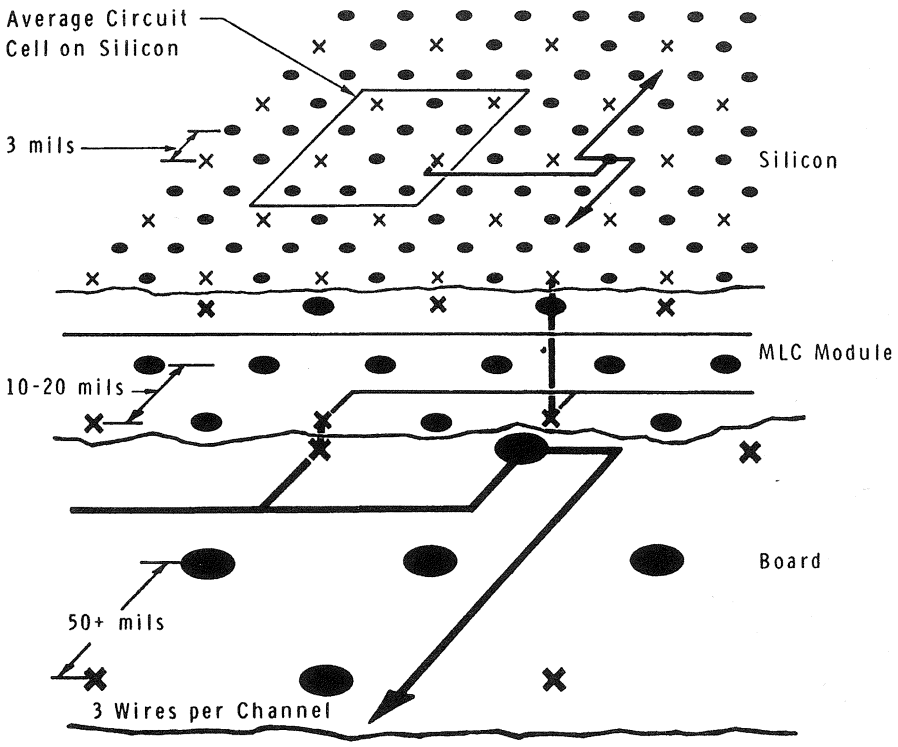


FIGURE 35 Grid reductions, showing the silicon chip, MLC module and printed circuit board.

1.6.3 Hermetic Seals

Metal-ceramic adhesion is produced by the wetting of the Mo or W by the glassy phases in the ceramic. Strong bonds are achieved when the ceramic is saturated with the lowest oxide of the metal. An additional requirement for good adhesion is the formation of a very low strain energy interface between the ceramic and metal, which is affected by the difference in their thermal expansions and the ductility of the metal. Mechanically rough surfaces can also add to the bond strength by providing more area for adhesion.

The TCM sealing arrangement is shown in Fig. 36. The flange is brazed with a gold-tin alloy to a Mo-Ni-Au metallized perimeter band on the substrate. The hermetic enclosure is completed with a tightly clamped C ring, and the enclosure is filled with helium gas, which is used to enhance the thermal conductivity of the module.

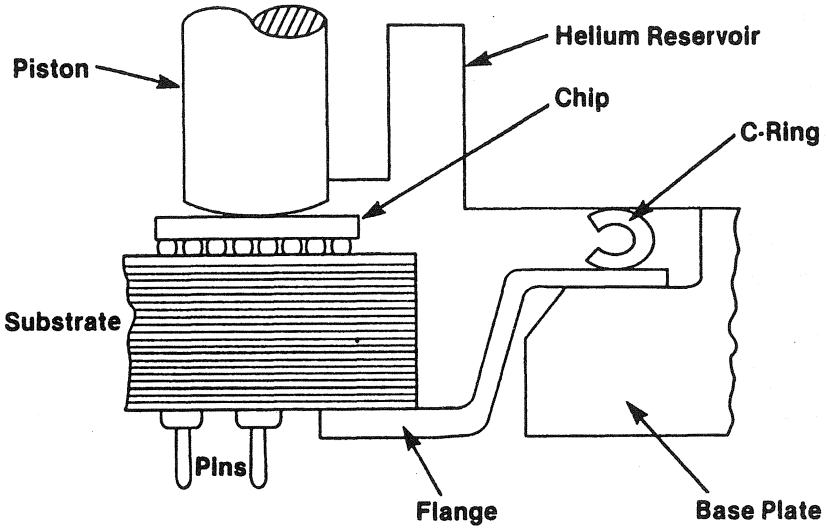


FIGURE 36 TCM module cross section, showing the pins, substrate, chip, piston, helium reservoir, C-ring and base plate.

The newer version of the TCM eliminates the flange and the enclosure is clamped directly to the bare ceramic, which is used in the new 309X computer systems. This module has the added advantage of eliminating several of the components in its structure. The specifications for this module are given in Table 1.

1.6.4 Cooling

SLT, MST, and MC modules transferred heat out of the chips through the solder pad interconnections to the substrate. Making the solder pads diameters larger and heights shorter to increase the cooling will tend to aggravate the fatigue problem. Therefore, the new 36 chip MCM and the TCM had to develop a new method for removing the heat.

The 36 chip MCM has a unique cooling arrangement, as shown in Fig. 33. This module has the ability to dissipate up to 85 W by the combination of substrate and backside cooling from the chip.

The TCM, therefore, had to implement a completely new cooling system, as reported by Chu et al. (1982) and Oktay and Kammerer

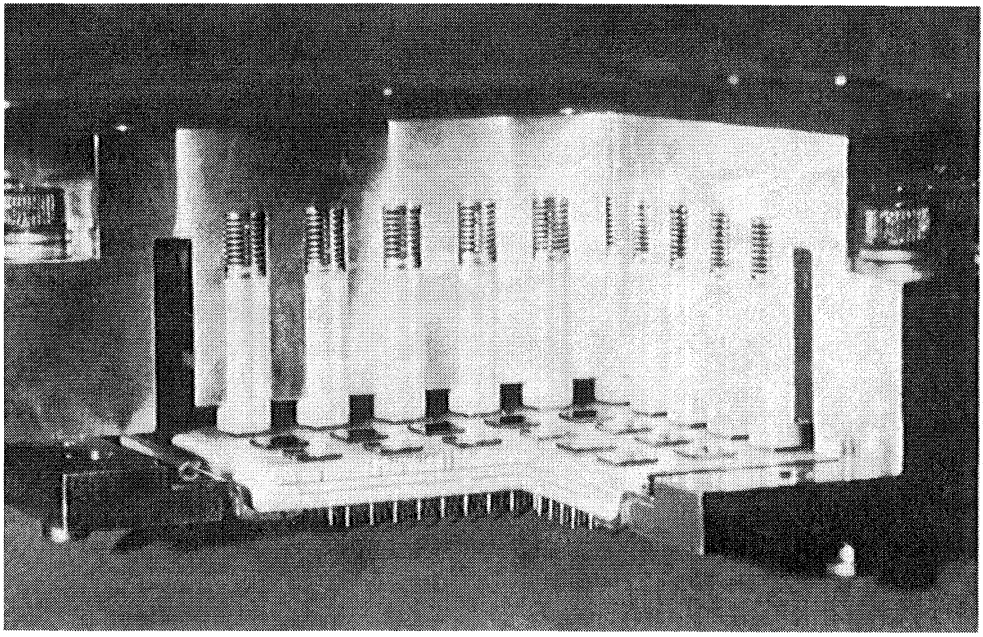


FIGURE 37 TCM cross-section, showing pistons, chips, substrate and flange.

(1982). The heat is now removed from the back of the chips, as shown in Figs. 37 and 38. Each chip is contacted by a separate spring-loaded aluminum piston when the cover is in place. The heat produced in the chip is conducted by contact to the piston and through the helium gas fill. The hermetic seal is needed to contain the helium gas. The pistons have a thermal resistance of 4.4 °C/W and the helium gas 3.5 °C/W, for a total of 7.9 °C/W, which is an acceptable value. Cooling water flows into the channels in the exposed cover to remove the heat from the chips. These modules can dissipate up to 300 W, and therefore, cooling the chips directly allows a much wider choice of ceramics from which selections can be made.

1.6.5 Input/Output Pins

There are 1800 pins brazed to the bottom surfaces of the TCM modules, which represents a means for interconnecting and powering each chip. These pins are brazed with the same gold-tin alloy used to braze the